INTRODUCTION

The ELEC4609 term project is to design a pseudorandom bicycle taillight controller using dynamic logic. For this project, the dynamic pseudorandom sequence generator (PRSG) will be broken down into blocks: Shift Register, Master Clock Generator, 2-Phase Clock Generator, XNOR with Reset and Open Drain Output Buffer. The design will use a shift register is composed of five cascaded D flip-flops with feedback, which will generate a random sequence of repeating 31 bits (25 – 1 bits). The design must also provide solution to preventing a locked state of “1s” occurring in the sequence. Hence, the shift register will use an XNOR gate to force the PRSG low using a reset input. The shift register will require an astable input. Thus, the design must implement 2-phase clock generators, to sequence a non-overlapping waveform, with a waveform input by master clock. The master clock will use a capacitor (Cexternal) between 10nF to 500nF size, as such to generate a viewable frequency sequence of 10Hz. The bicycle taillight must operate on two AA batteries, or 3V input, with the LED having a 2V and 10mA rating requirement. Subsequently, the designs output buffer transistor must be able to drain 1V VDS and 3V VGS, and sink 10mA. Furthermore, all of these designed blocks must fit on a 240Λ length by 230Λ width, with six probe pads using space of 40Λ length by 40Λ width; Λ = 2.4um.

System Level Block

The Dynamic Pseudorandom Sequence Generator is composed of Shift Register, Master Clock Generator, 2-Phase Clock Generator, XNOR and Output Buffer blocks.

Shift Register

The D flip-flop takes in non-overlapping Φ1 and Φ2 input from the 2-phase clock generator. When the Φ1 is a logic high, the flip-flop stores the input, and when Φ2 is a logic high, the flip-flop outputs the data. Figure X shows a D flip-flop cell designed using nMOS and pMOS (M1, M3 and M2, M4), and two double transmission gate nMOS layout (M5, M6). The reason for using nMOS for M5 and M6, is due to it having lower channel leakage, and can be further reduced using longer MOSFET, hence the use of double T-gates. The shift register is built using five cascaded D flip-flops using feedback as shown in figure X. This block serves to generate and output a random waveform. Since the block uses five D flip-flops, the random repeating sequence is 31 bit long (25 - 1).

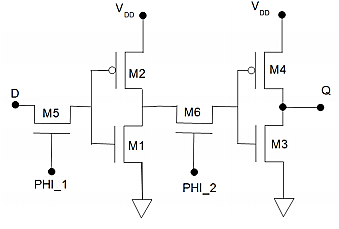


Figure 1: D Flip-Flop Circuit

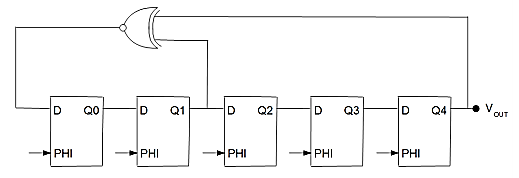


Figure 2: Shift Register Circuit

Master Clock Generator

The master clock generator is used to create an astable oscillating waveform. This block uses external capacitor to generate a clock signal, Φ. The sequence is adjusted to be roughly 10Hz, by setting the Cexternal between 10nF and 500nF. Shown in Figure X, is an implementation of the master clock generator.

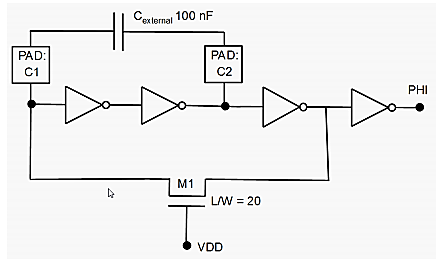


Figure 3: Master Clock Generator Circuit

2-Phase Clock Generator

The 2-phase clock generator serves to generate a two non-overlapping sequences Φ1 and Φ2 by using the Φ clock output from the master clock generator. These two signals are then used to drive the D flip-flop, therein, drive the shift register. A possible configuration of the 2-phase clock generator is shown below in Figure X, however the Figure X setup is used. With the extra inverters, the system makes sure that Φ1 and Φ2 are never simultaneously high, and the overlap does not occur midrail.

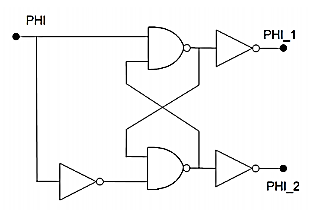


Figure 4: 2-Phase Clock Generation Circuit

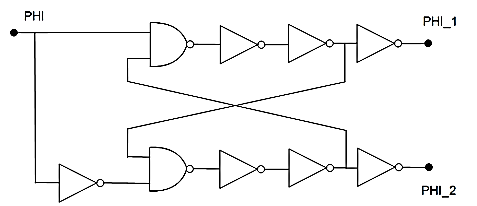


Figure 5: 2-Phase Clock Generation with addition Inverters Circuit

XNOR Gate

The PRSG uses the XNOR gate with RESET, to assert and force its output to logic low; the block performs a XNOR operation with RESET. The gate is used to prevent the PRSG from entering a locked state, where all of the five D flip-flops have a logic high stored. A configuration of XNOR can be achieved by using five NAND gates, as shown below in Figure X. However, the problem of locked state will persist, as 1Ꚛ1 is 1. Therefore XNOR with RESET is designed using NANDs and NOR gates, and the configuration is shown below. The four NANDs are setup as such to create and XOR gate, and the addition of NOR creates a XNOR with reset functionality.

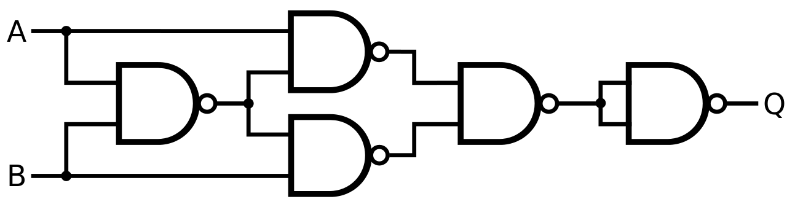


Figure 6: XNOR Gate Circuit

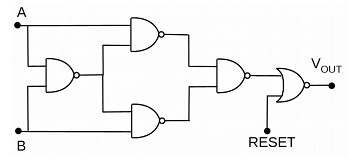
\

Figure 7: XNOR with RESET Gate Circuit

Output Buffer

The output buffer in PRSG is designed using one nMOS transistor, as shown below. The open drain setup of the nMOS serves to sink 10mA and 1V VDS and 3V VGS. The large buffer is used to drive the load and reduce the switching time. The output buffer could be made up of cascaded inverters, but that will increase the switching delay, and the size, hence, the nMOS transistor is used.

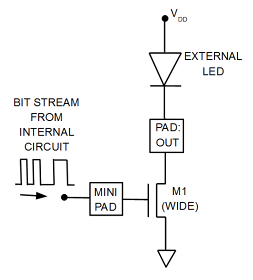


Figure 8: Output Buffer Circuit

INVERTER

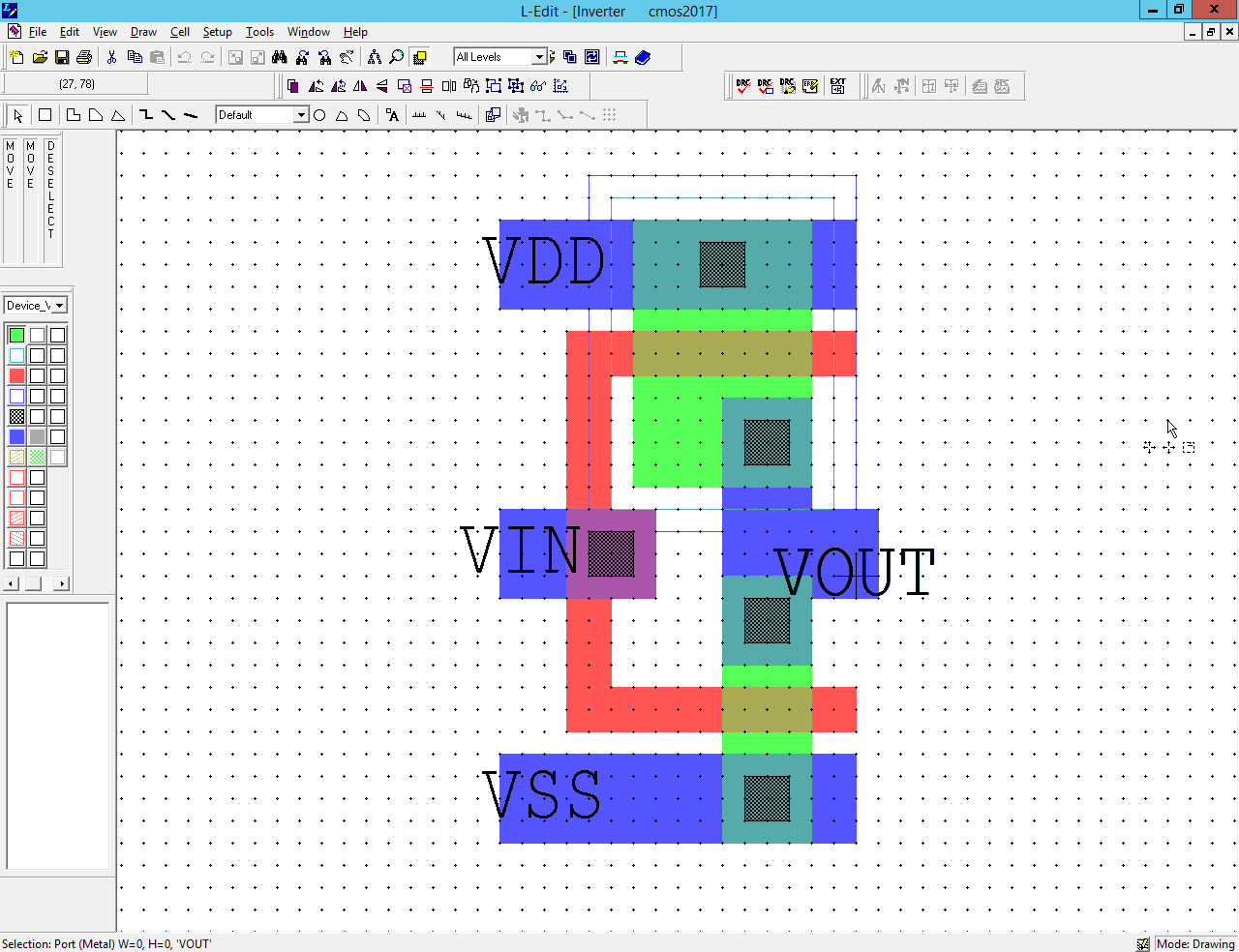
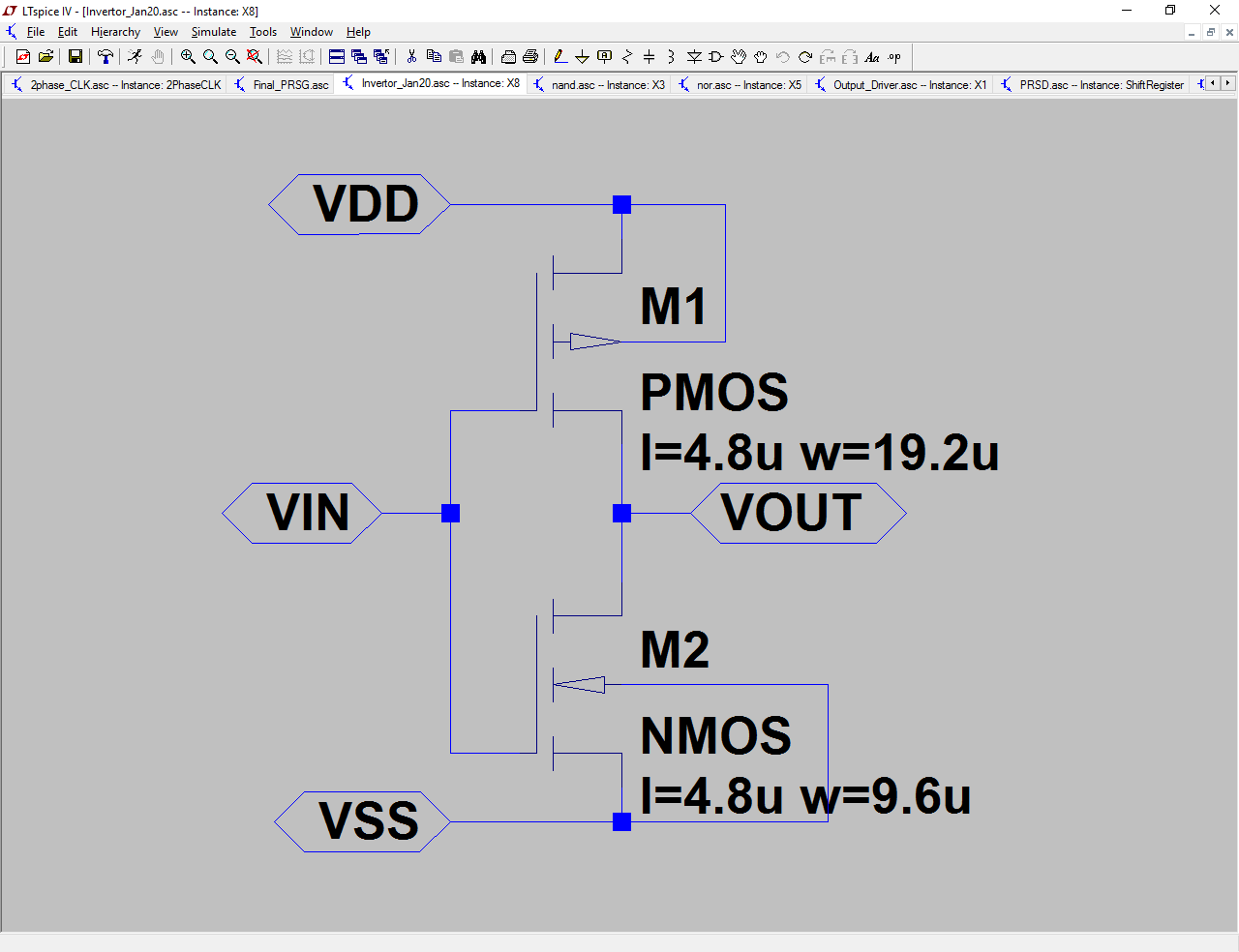


Figure 9: Invertor Schematic Figure 10: Invertor Layout

|  |  |
| --- | --- |
| VIN | VOUT = ~(VIN) |
| 0 | 1 |
| 1 | 0 |

Table 1: Inverter Truth Table

NAND

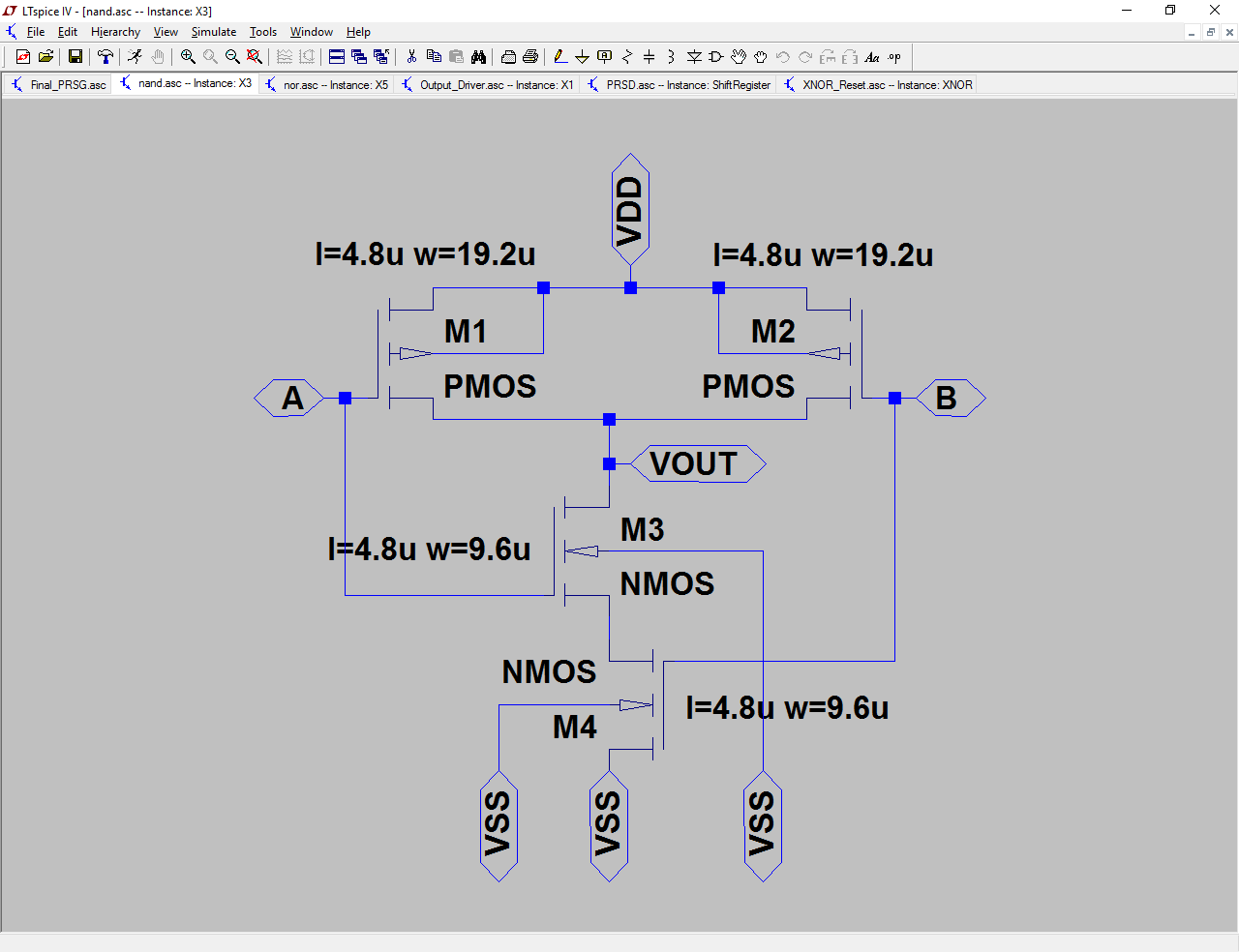
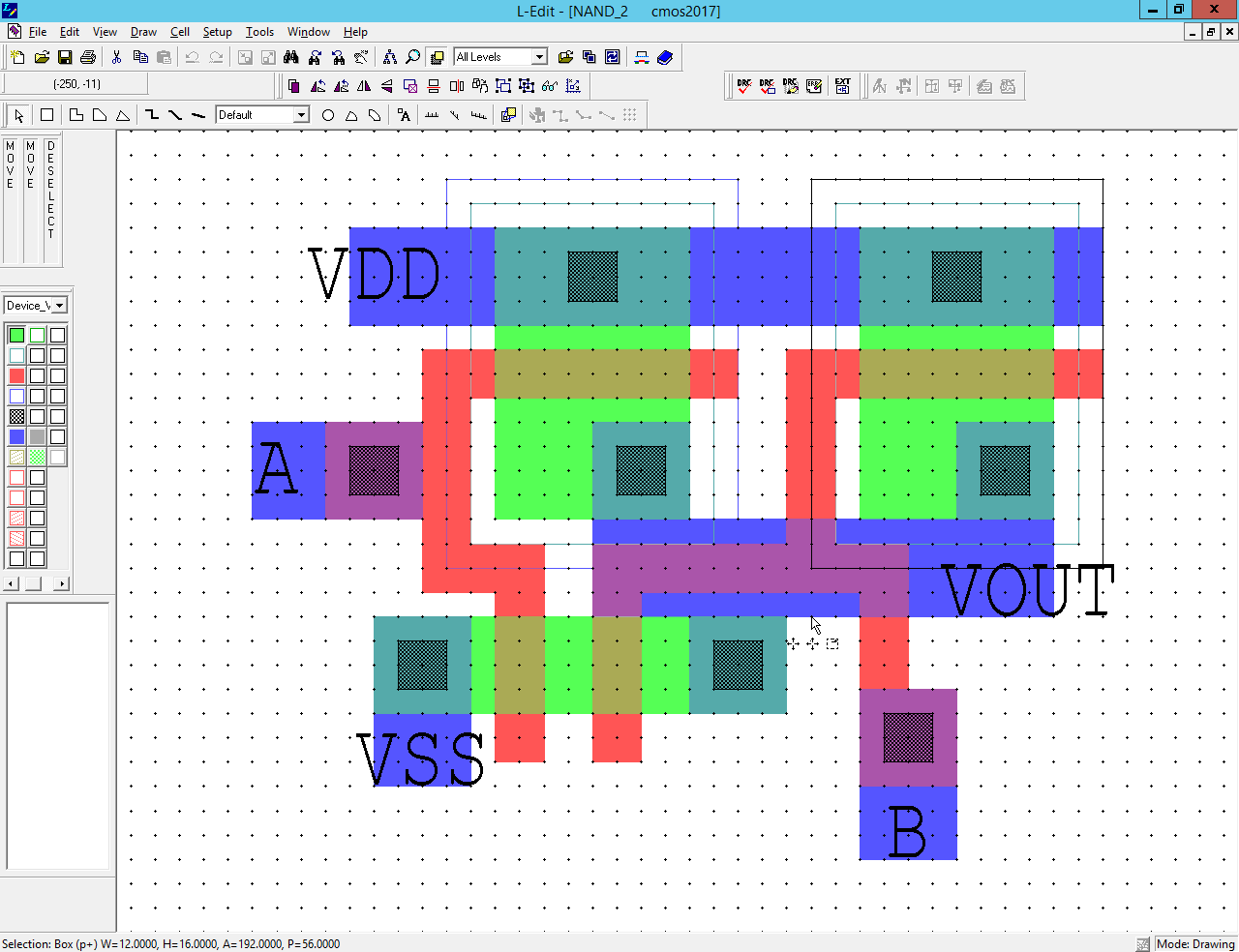


Figure 11: NAND Schematic



|  |  |  |
| --- | --- | --- |
| A | B | VOUT = ~(A∙B) |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Figure 2: NAND Truth Table

Figure 12: NAND Layout

NOR

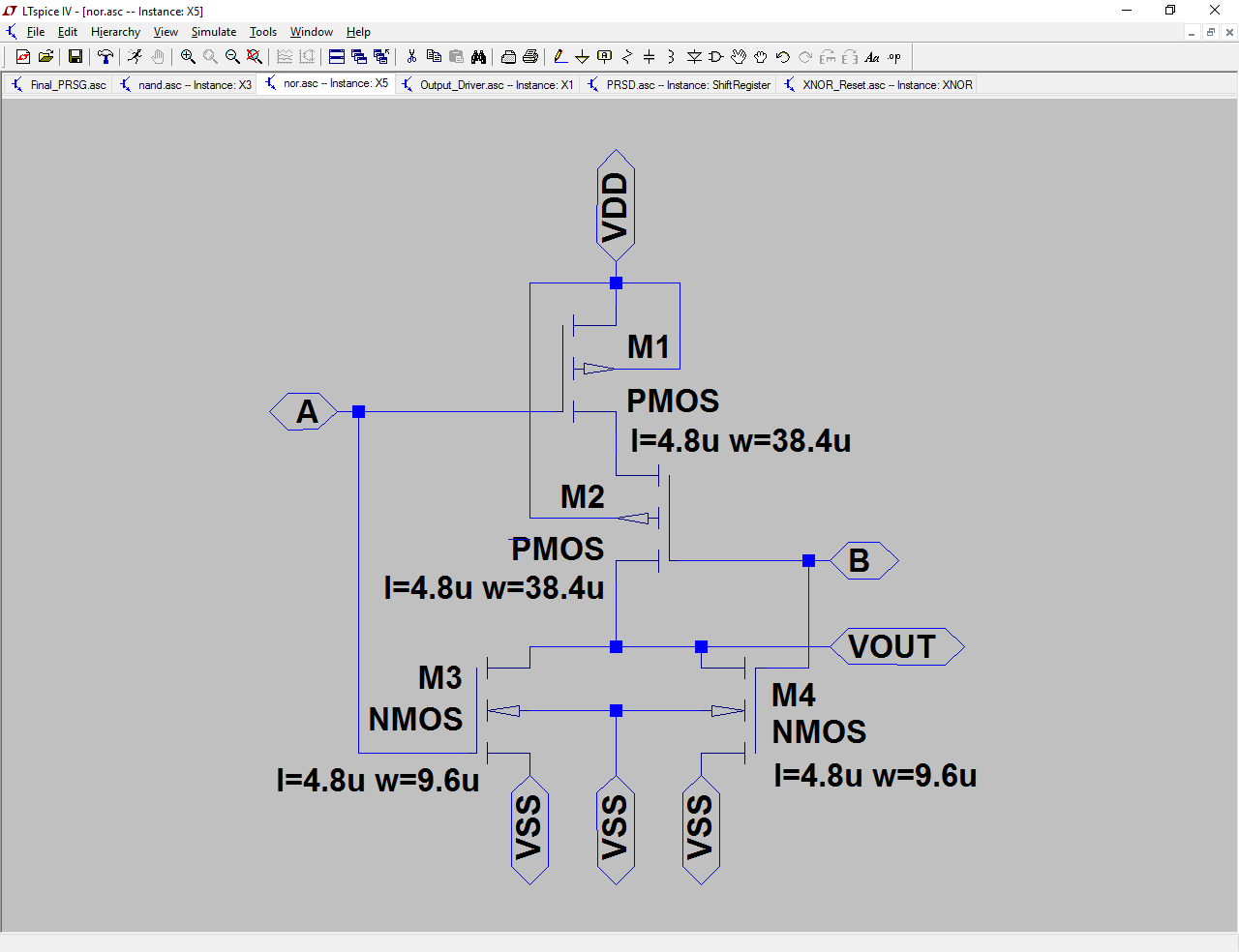


Figure 13: NOR Schematic

|  |  |  |
| --- | --- | --- |
| A | B | VOUT = ~(A+B) |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

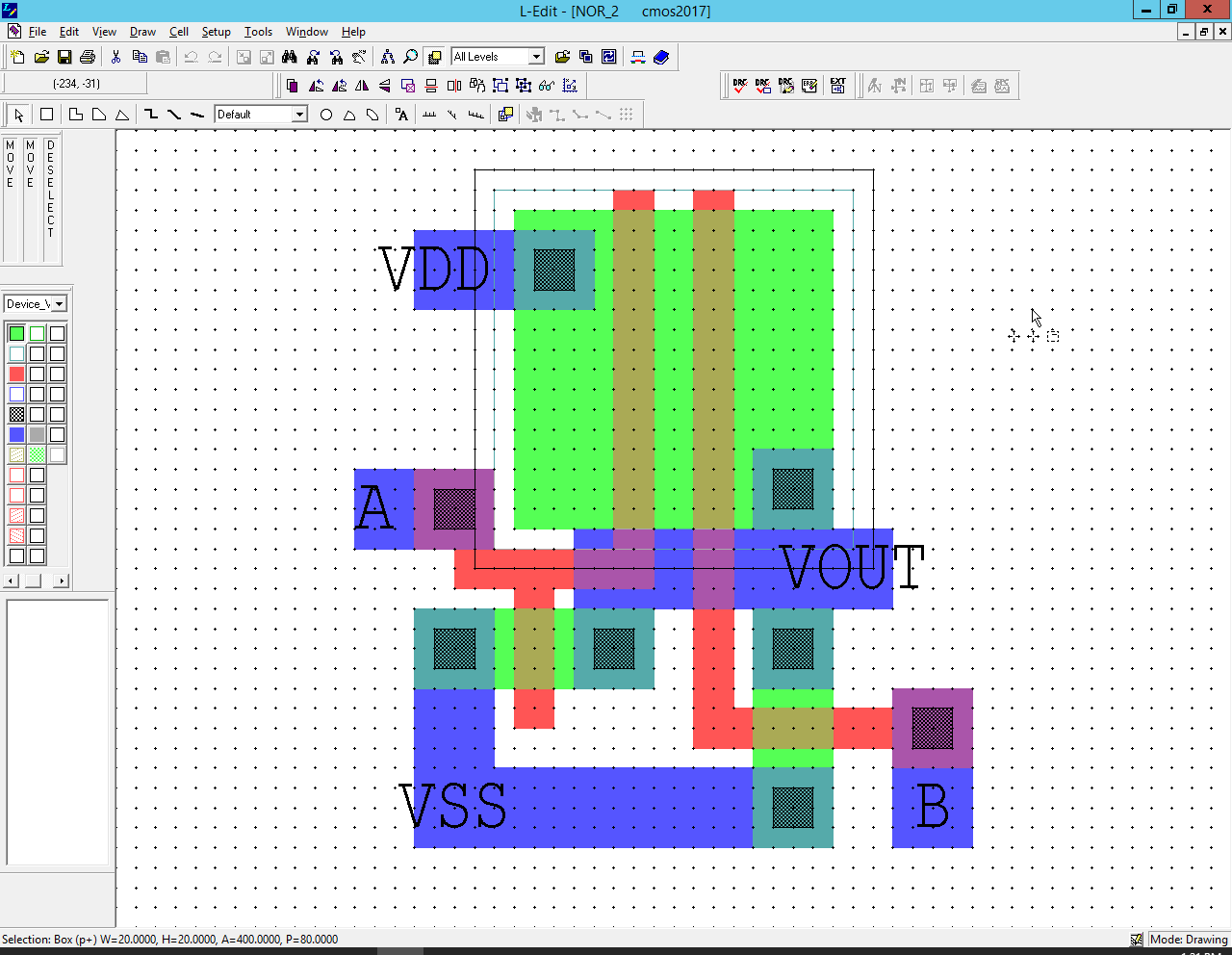


Table 3: NOR Truth Table

Figure 14: NOR Layout

XNOR

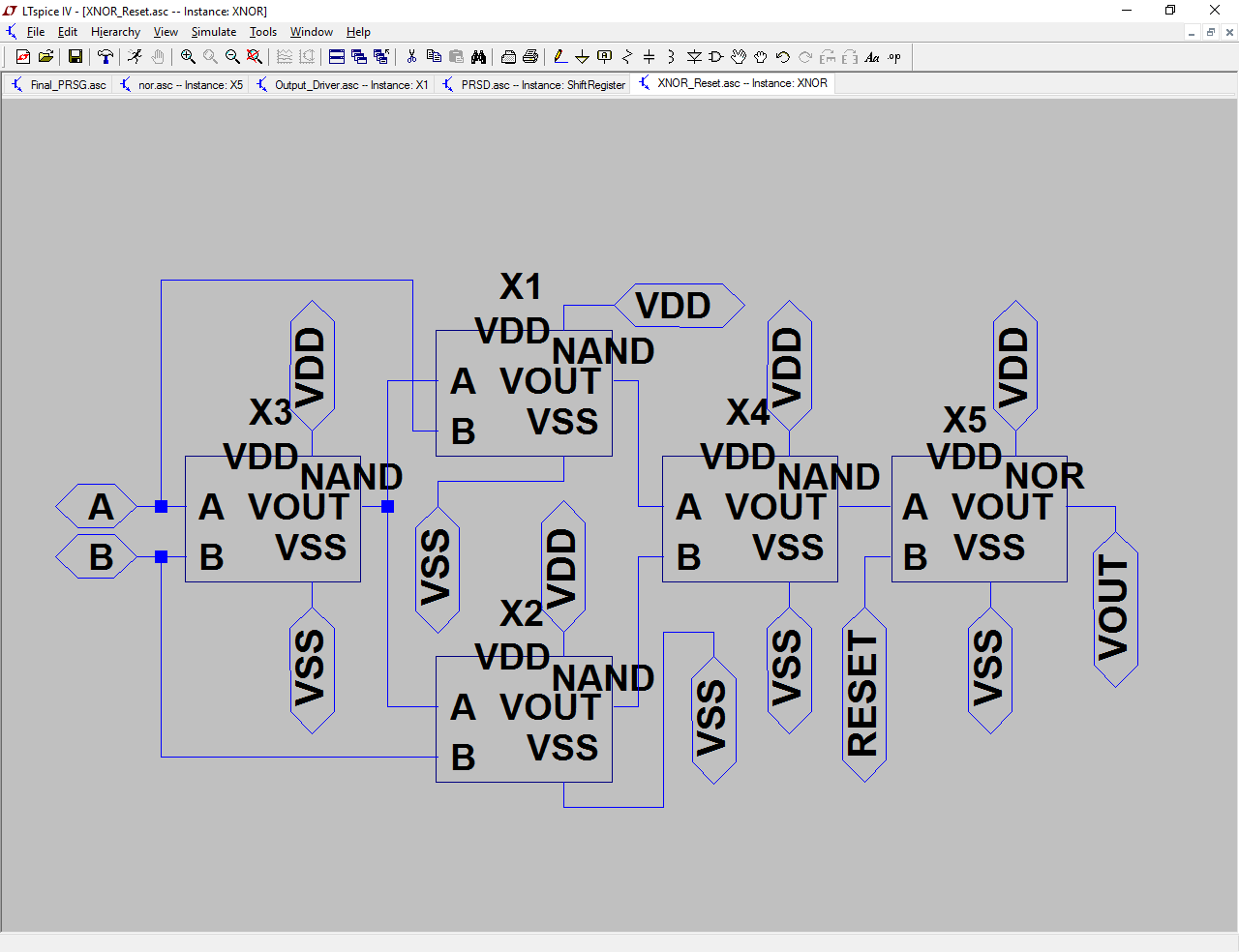


Figure 15: XNOR with Reset Schematic (Refer to NAND and NOR Schematics Figures for MOSFET L and W)

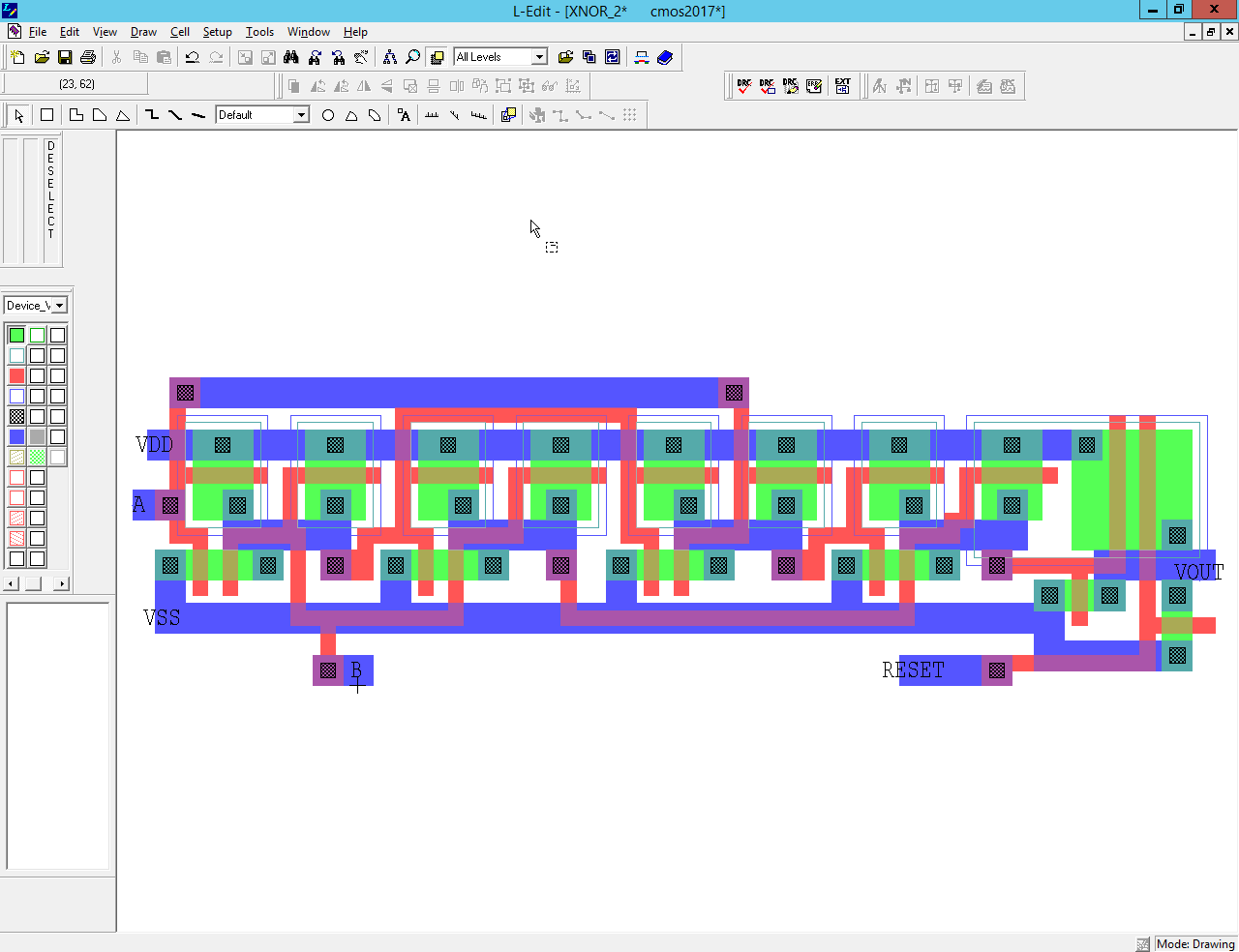


Figure 16: XNOR with Reset Layout

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | X = ~(A∙B) | Y = ~(A∙X) | Z=~(B∙X) | W=~(Y∙Z) | Reset | VOUT = ~(Reset+W) |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

Table 4: XNOR with Reset Truth Table

Master Clock Generator

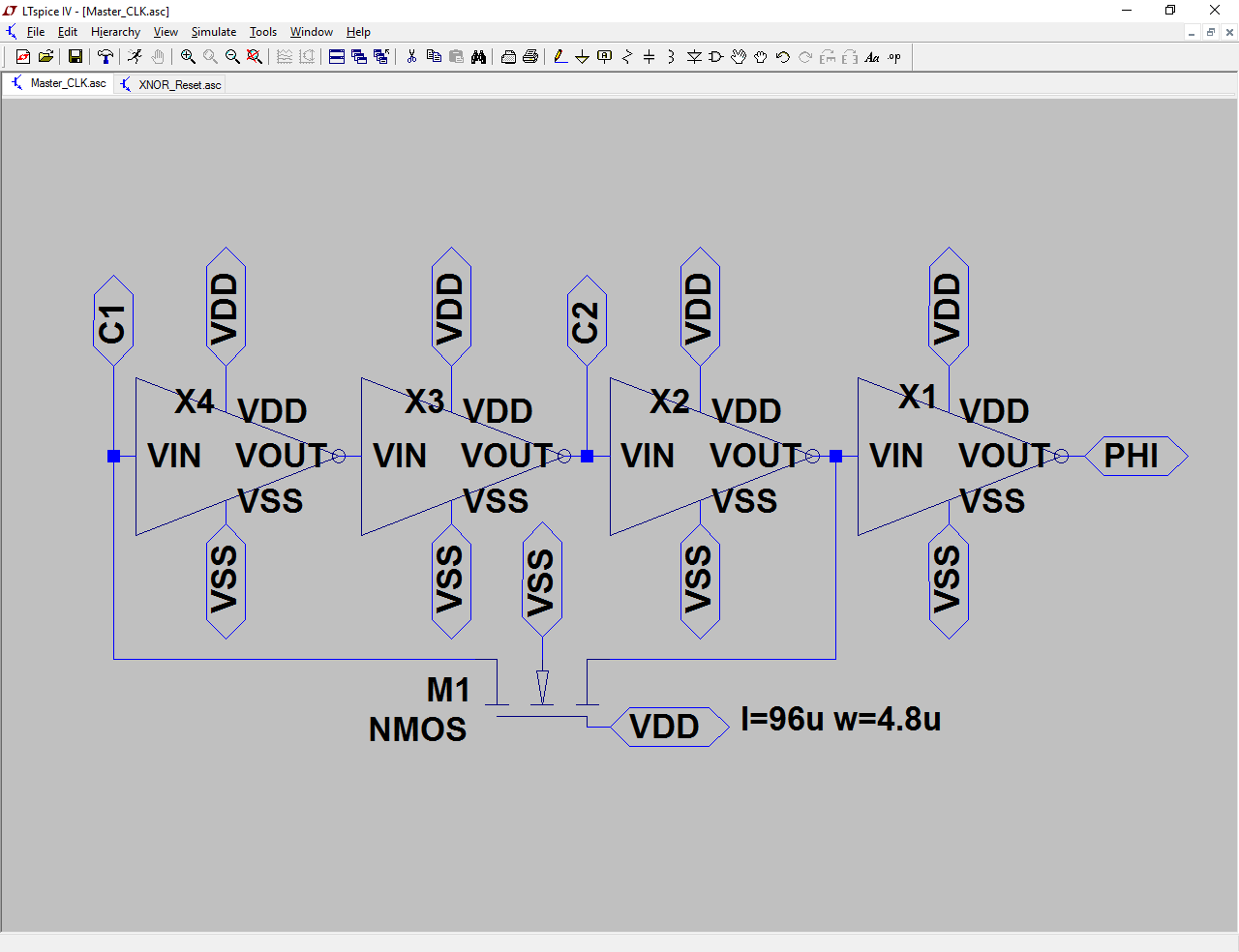


Figure 17: Master Clock Generator Schematic (Refer to Inverter Schematic Figure for MOSFET L and W)

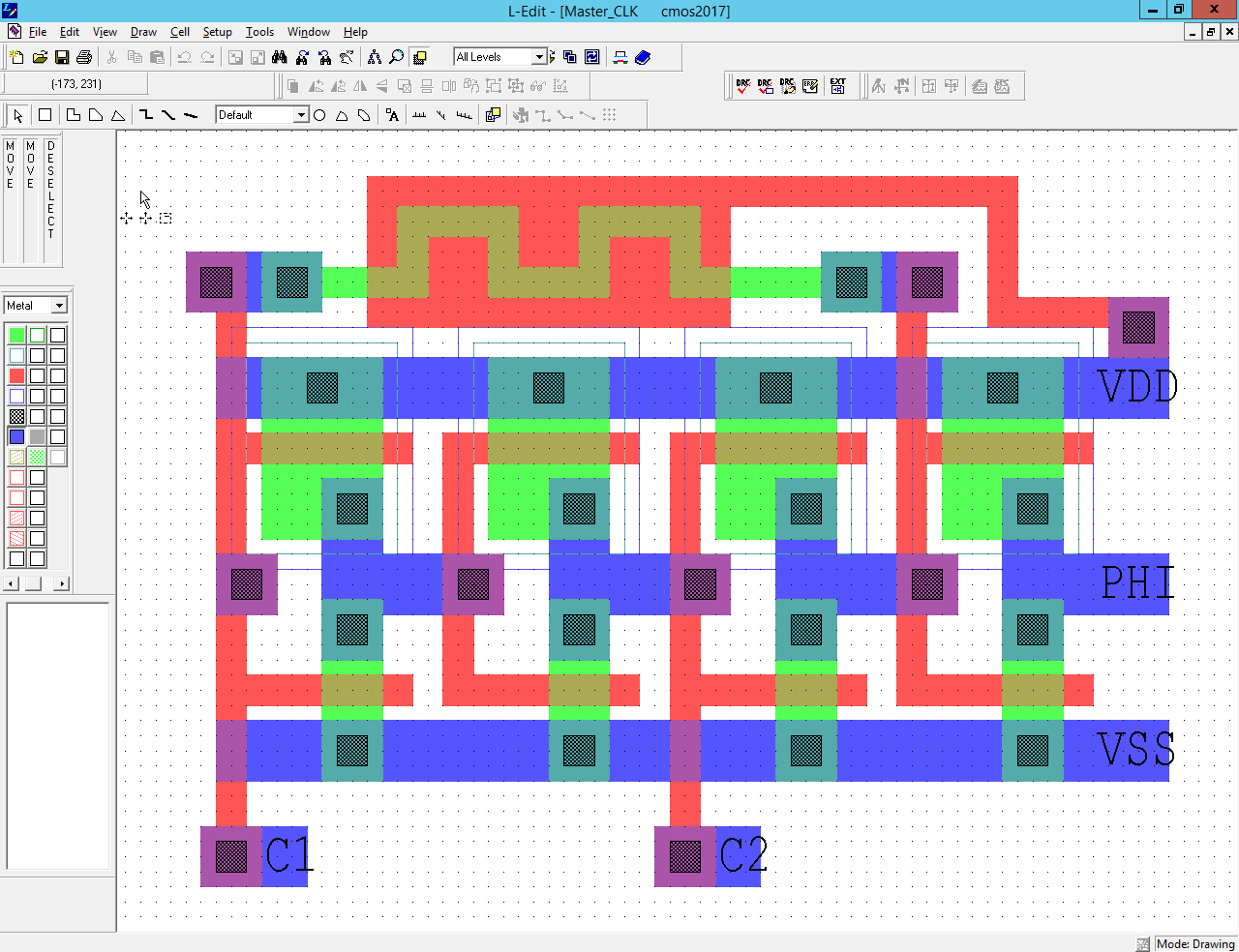


Figure 18: Master Clock Generator Layout

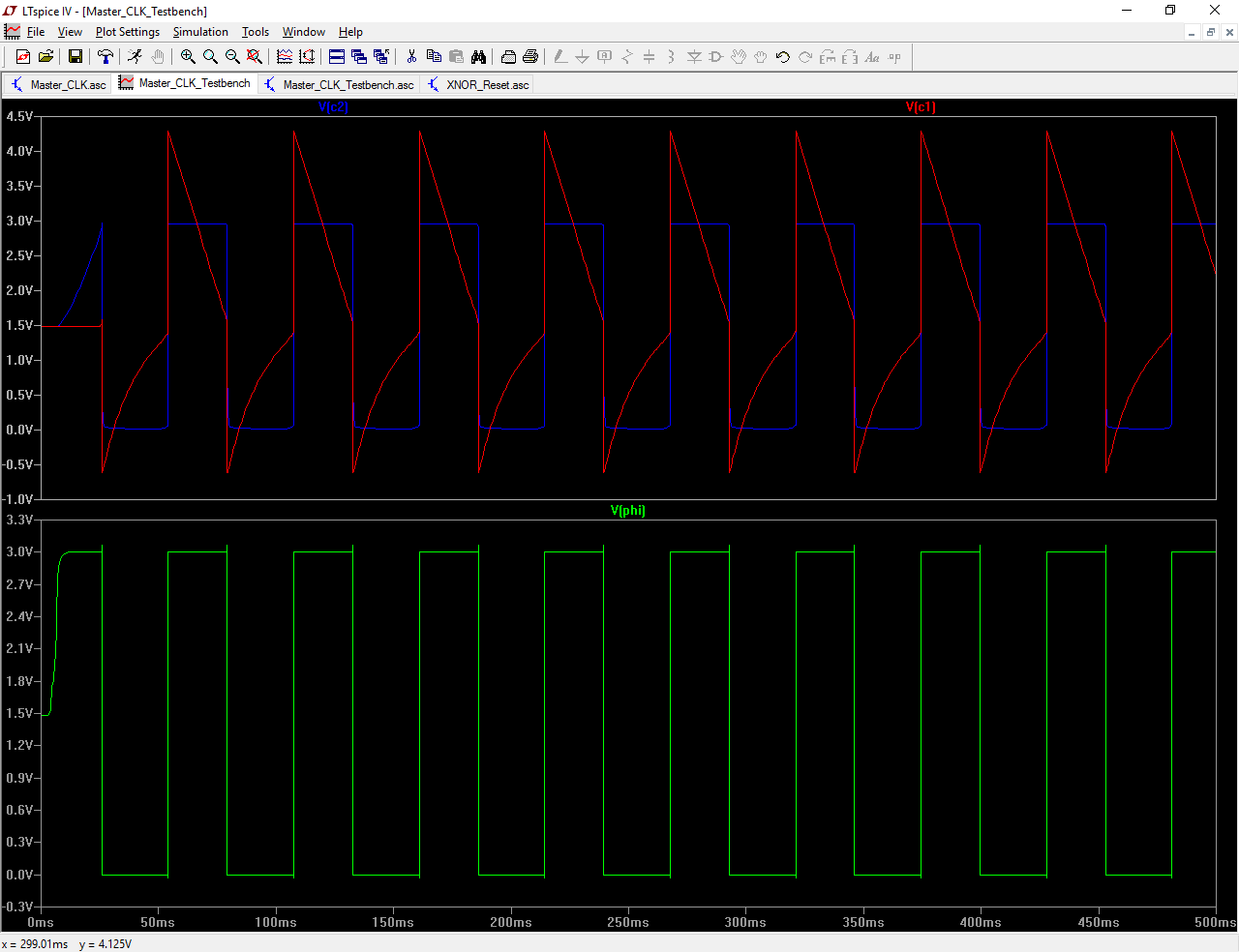


Figure 19: Master Clock Generator SPICE Simulation

2-Phase Clock Generator

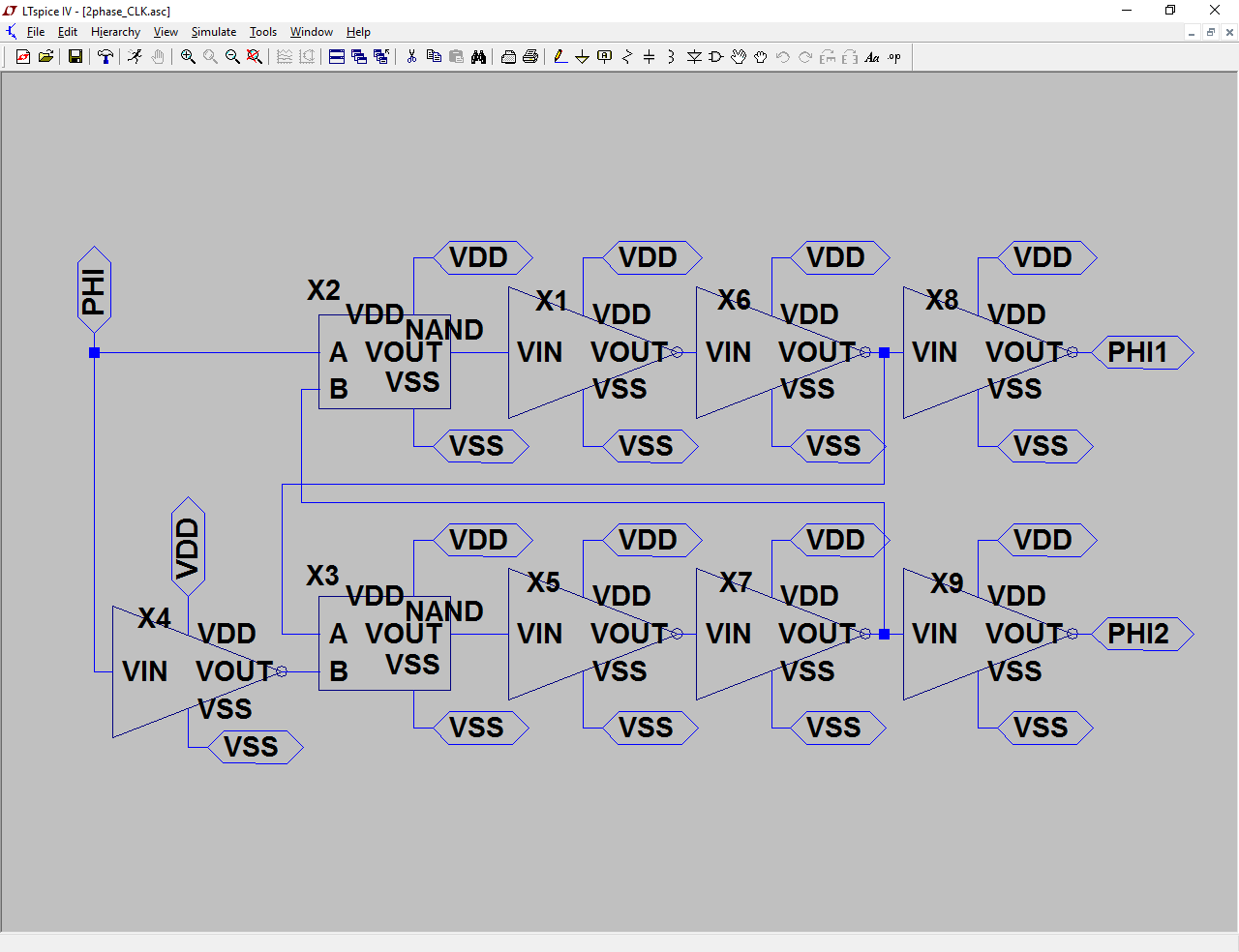


Figure 20: 2-Phase Clock Generator Schematic (Refer to Inverter and NAND Schematic Figures for MOSFET L and W)

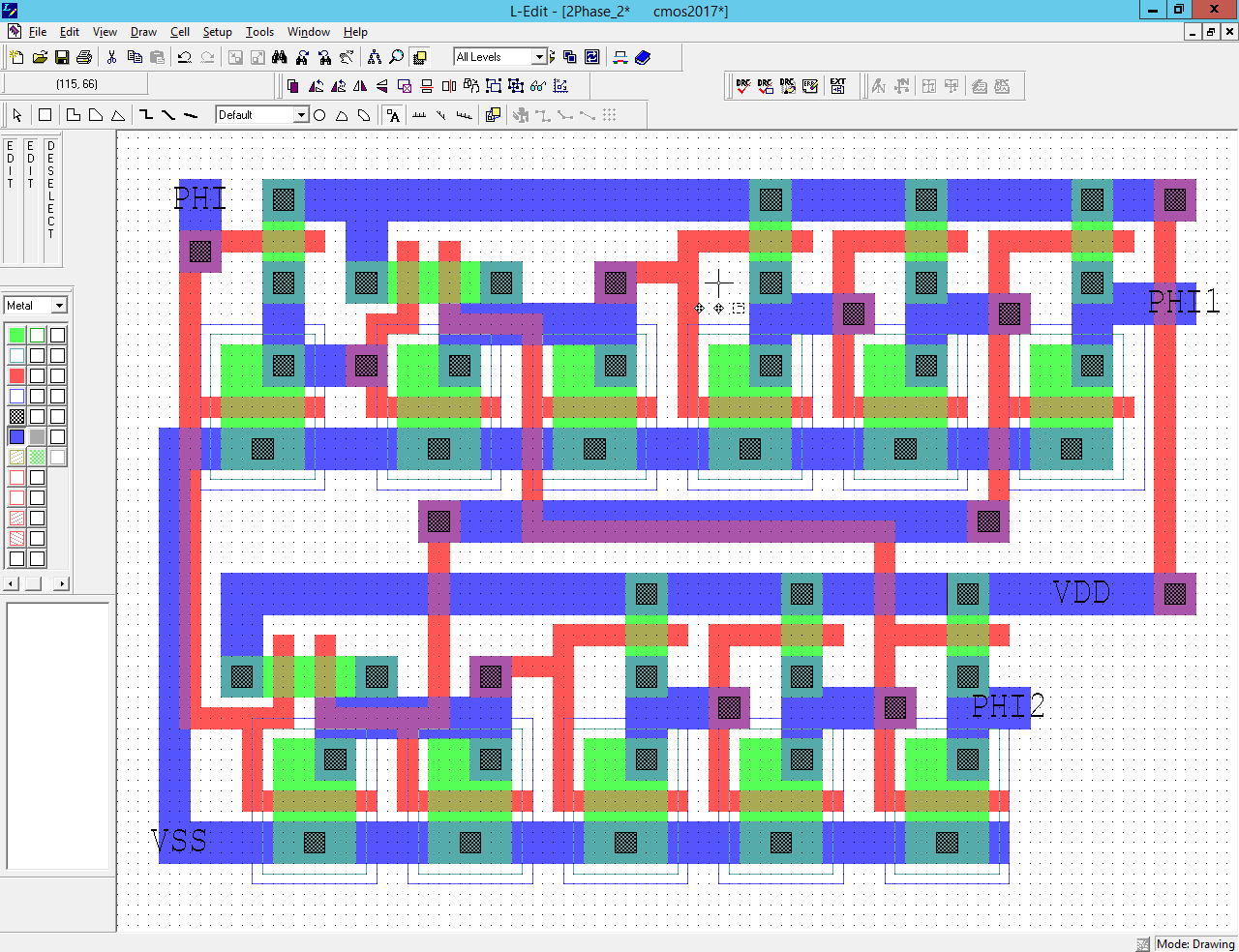


Figure 21: 2-Phase Clock Generator Layout

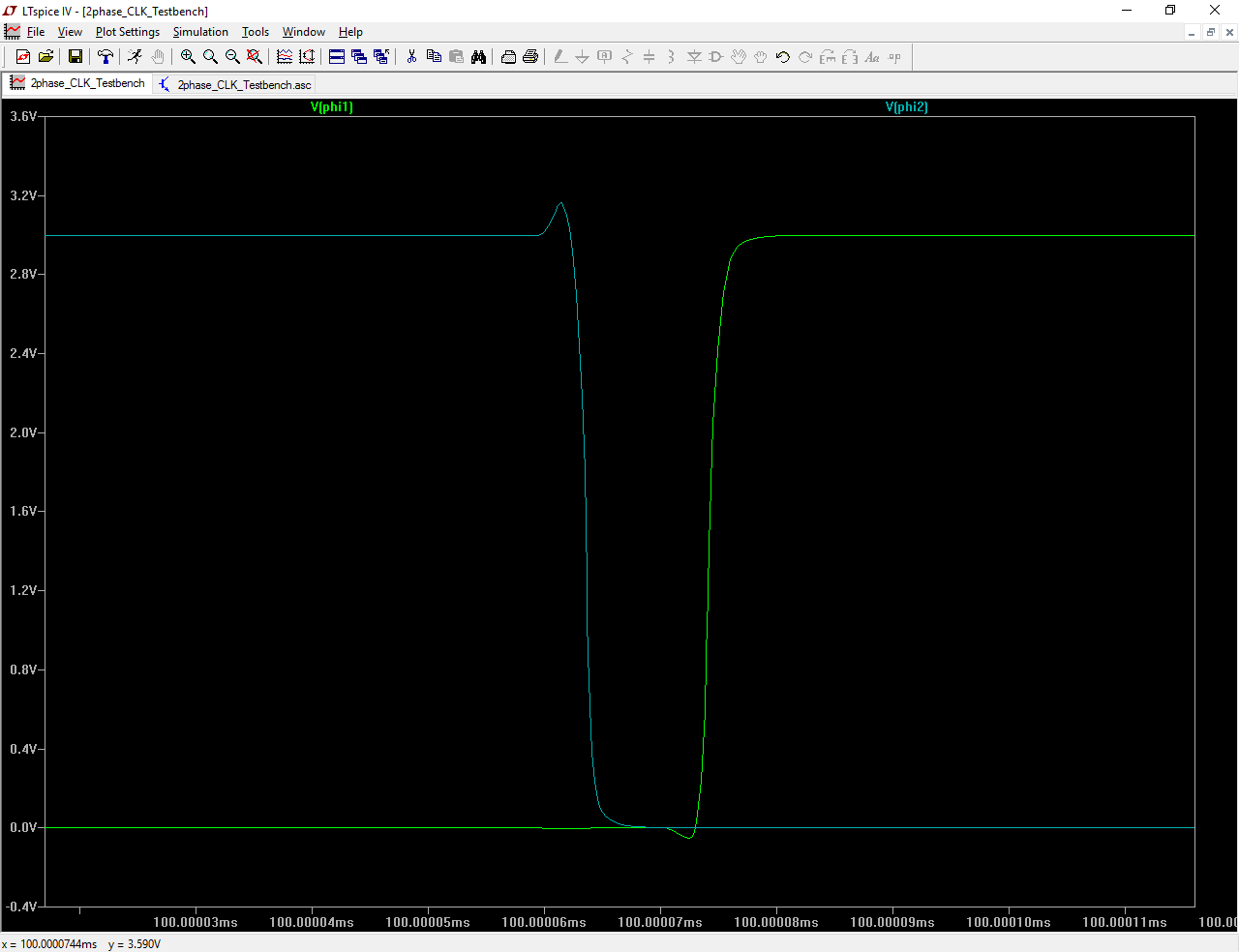


Figure 22: 2-Phase Clock Generator Overlap SPICE Simulation

It is important to minimize the overlap between Φ1 and Φ2 to prevent them from being the same logic state at any given time. A good practice would be to have both of the Φs switch either top of the rail or at the very bottom. Having it switch midrail could result in the D flip-flop considering them the same logic state.

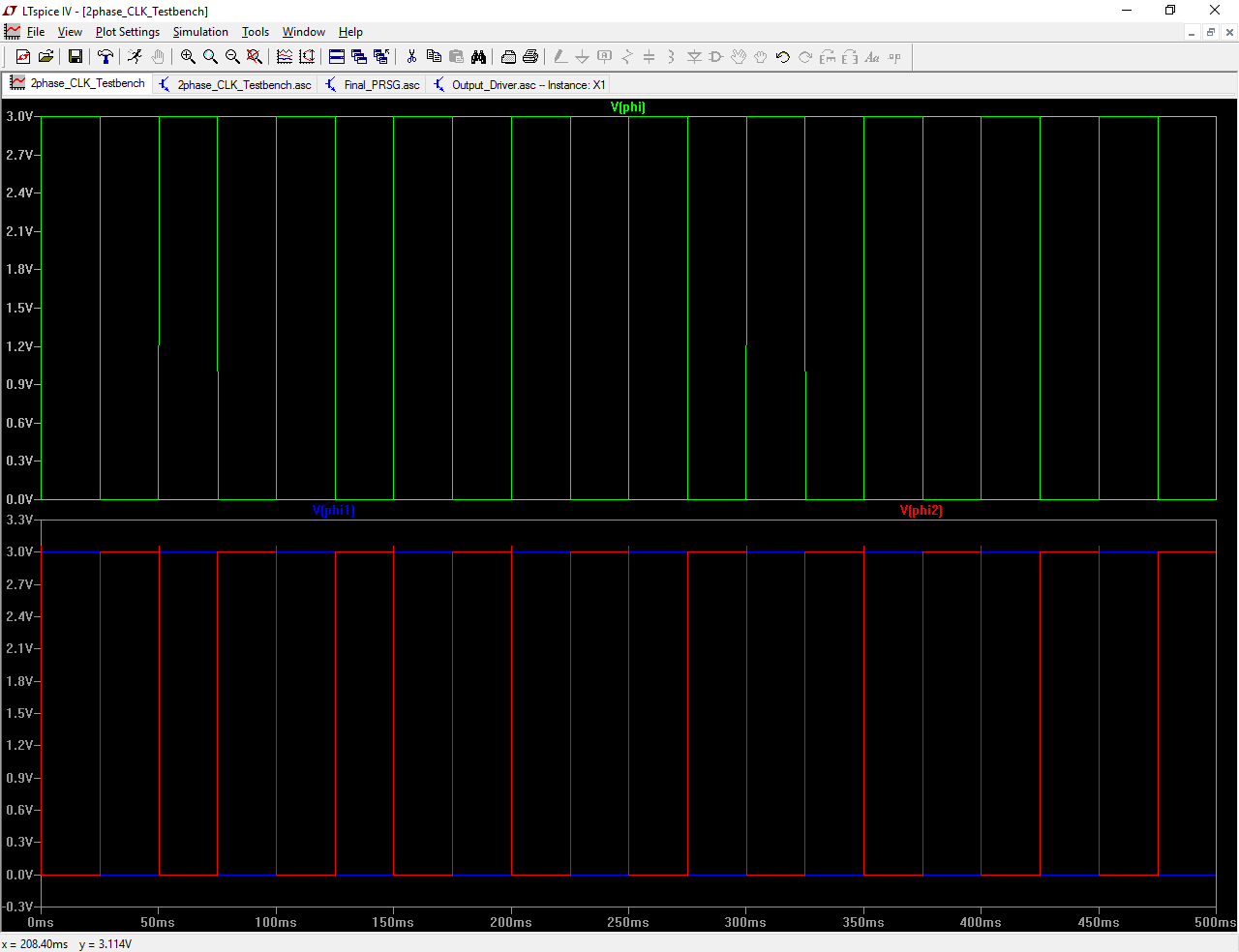


Figure 23: 2-Phase Clock Generator SPICE Simulation

D Flip-Flop

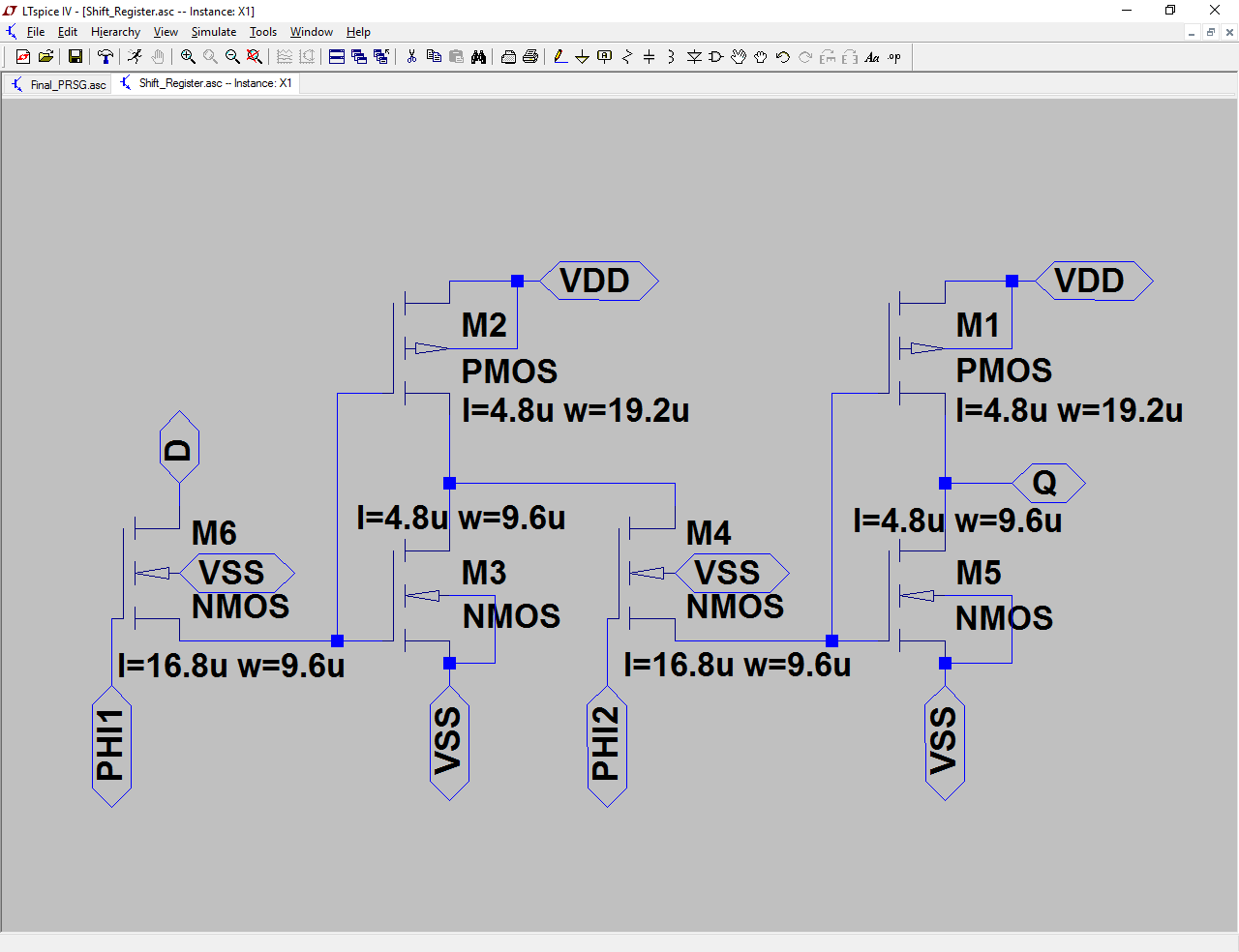


Figure 24: D Flip-Flop Schematic

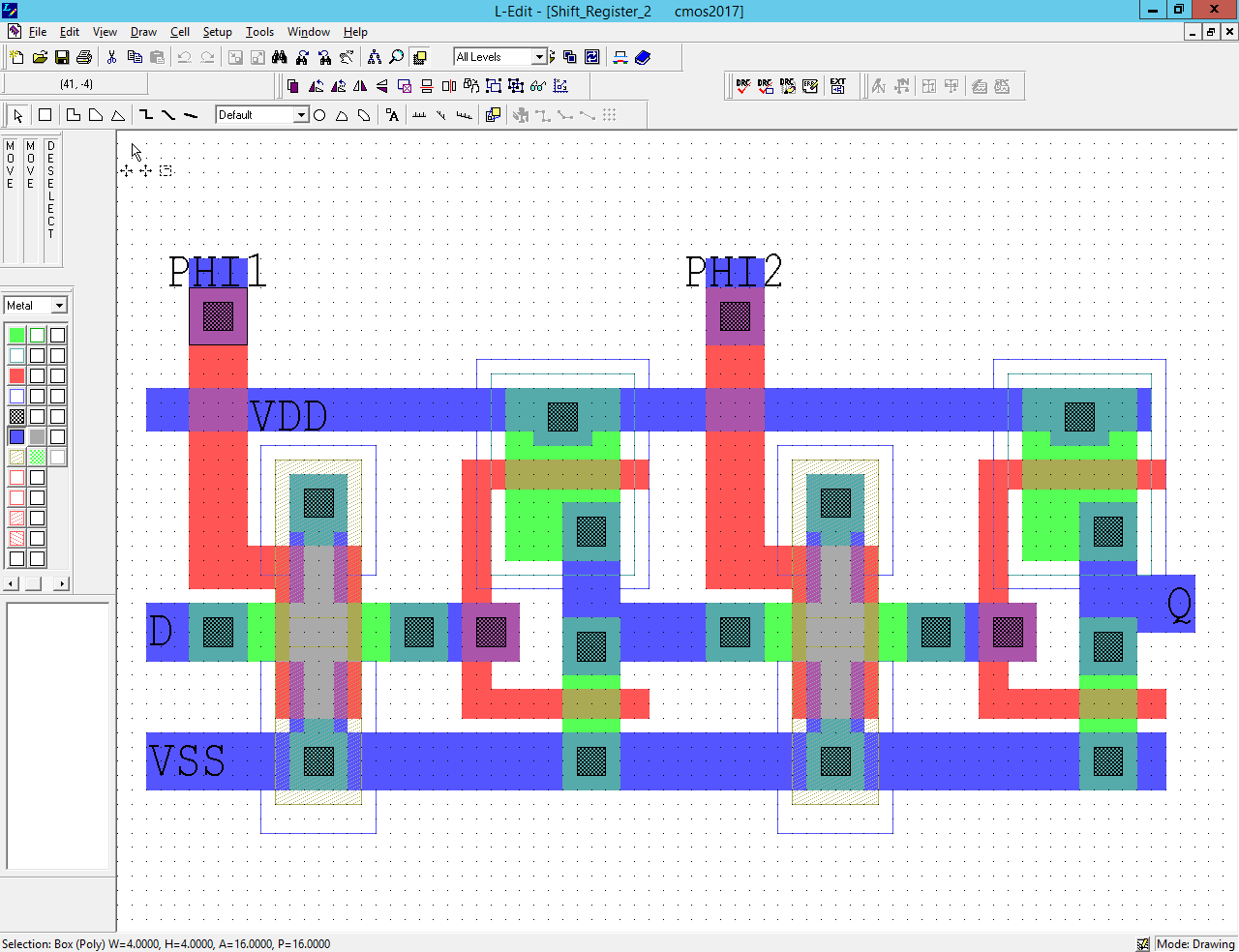


Figure 25: D Flip-Flop Layout

In the D flip-flop, the transmission gates are designed using nMOS. For the flip-flop, two nMOS double T-gates are used. The nMOS is minimizes leakage, as does the larger channel size double T-gate configuration; more beneficial than using pMOS. Subsequently, having a greater channel, means the length of the nMOS is also bigger; therefore, the circuit is also bigger.

Output Buffer

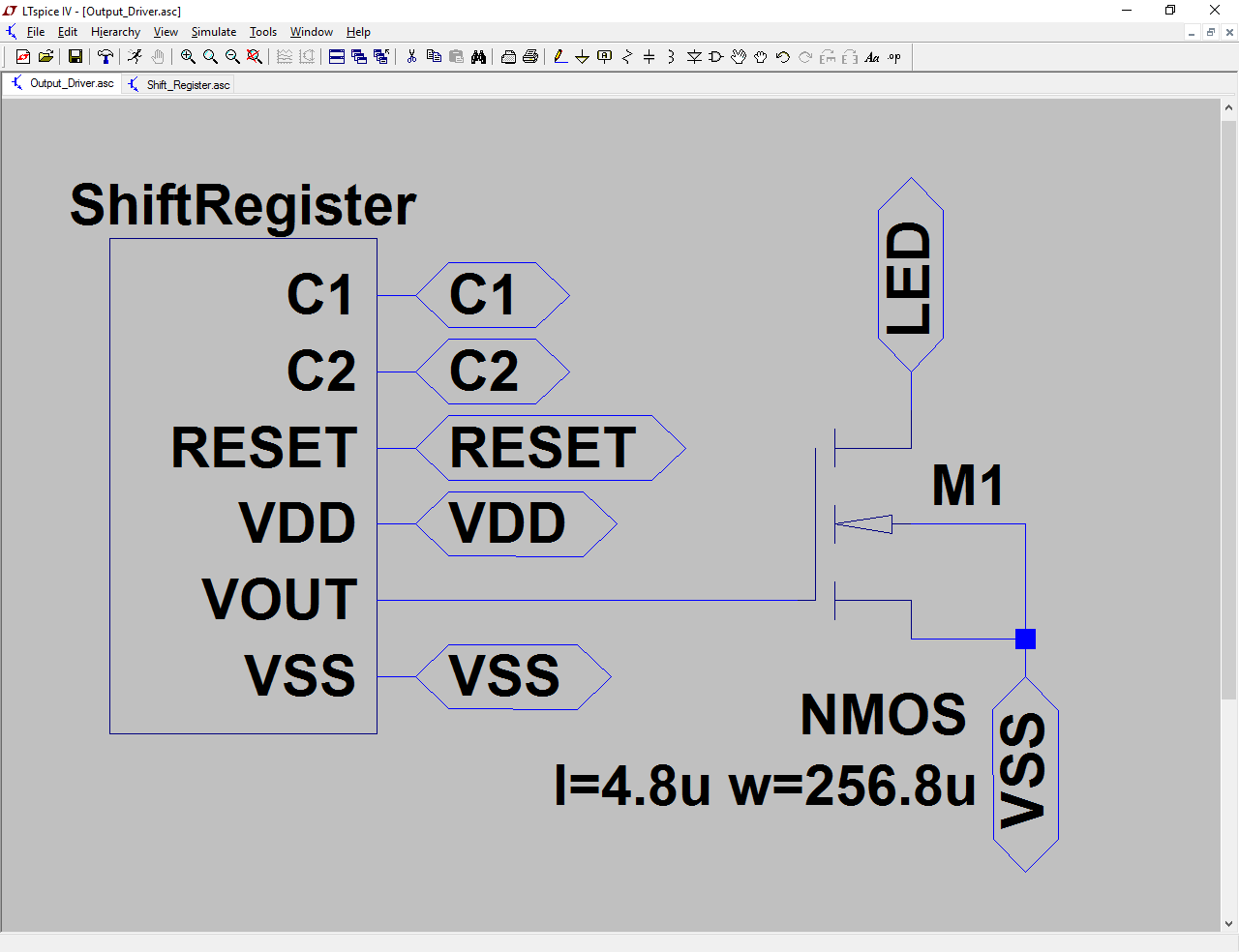
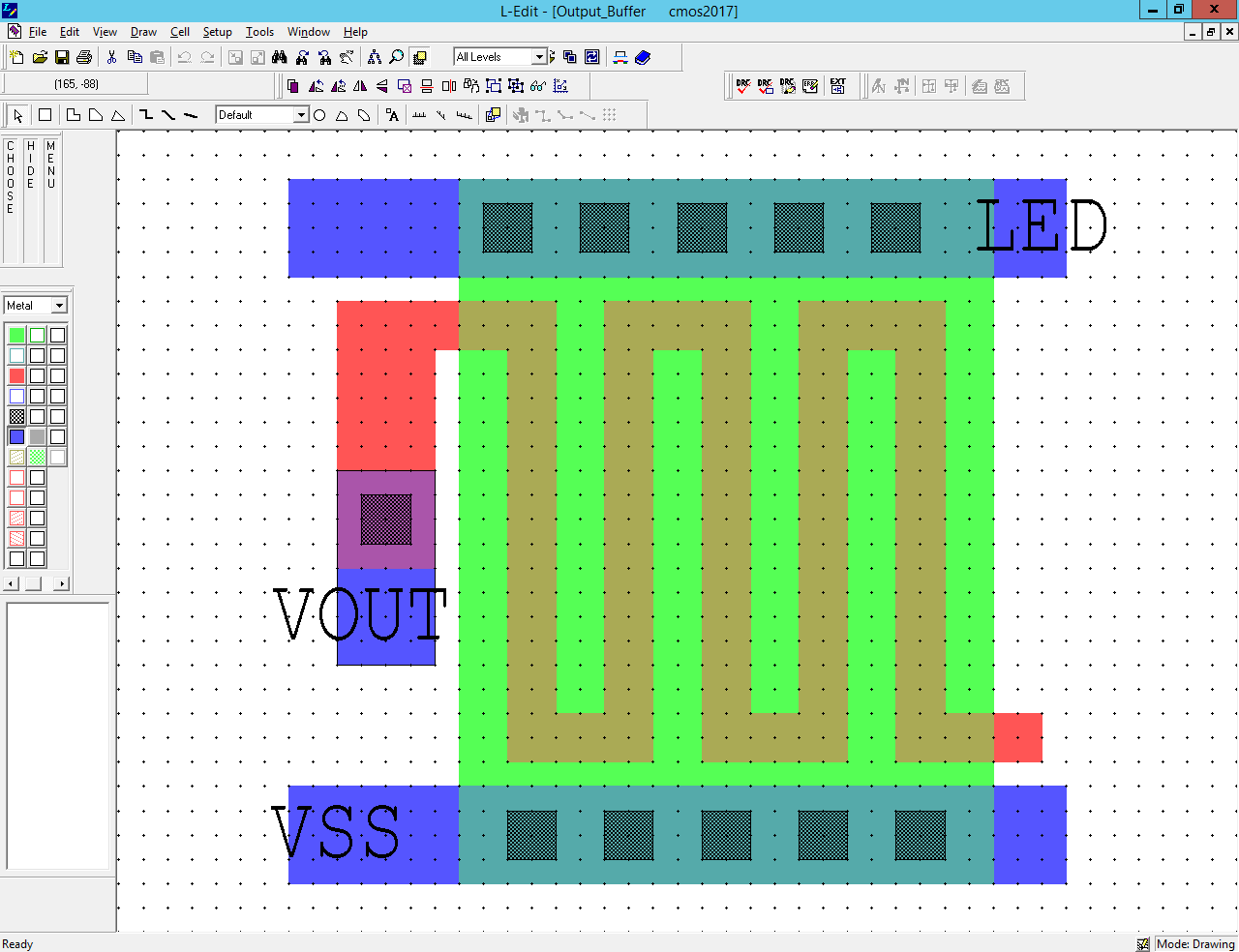


Figure 26: Output Buffer Schematic Figure: Output Buffer Layout

The output buffer has a very large transistor width to drive the large load. The width is 33 times larger than the length of the nMOS or larger. With a large width, an interdigitated or serpentine design is used.

PRSG

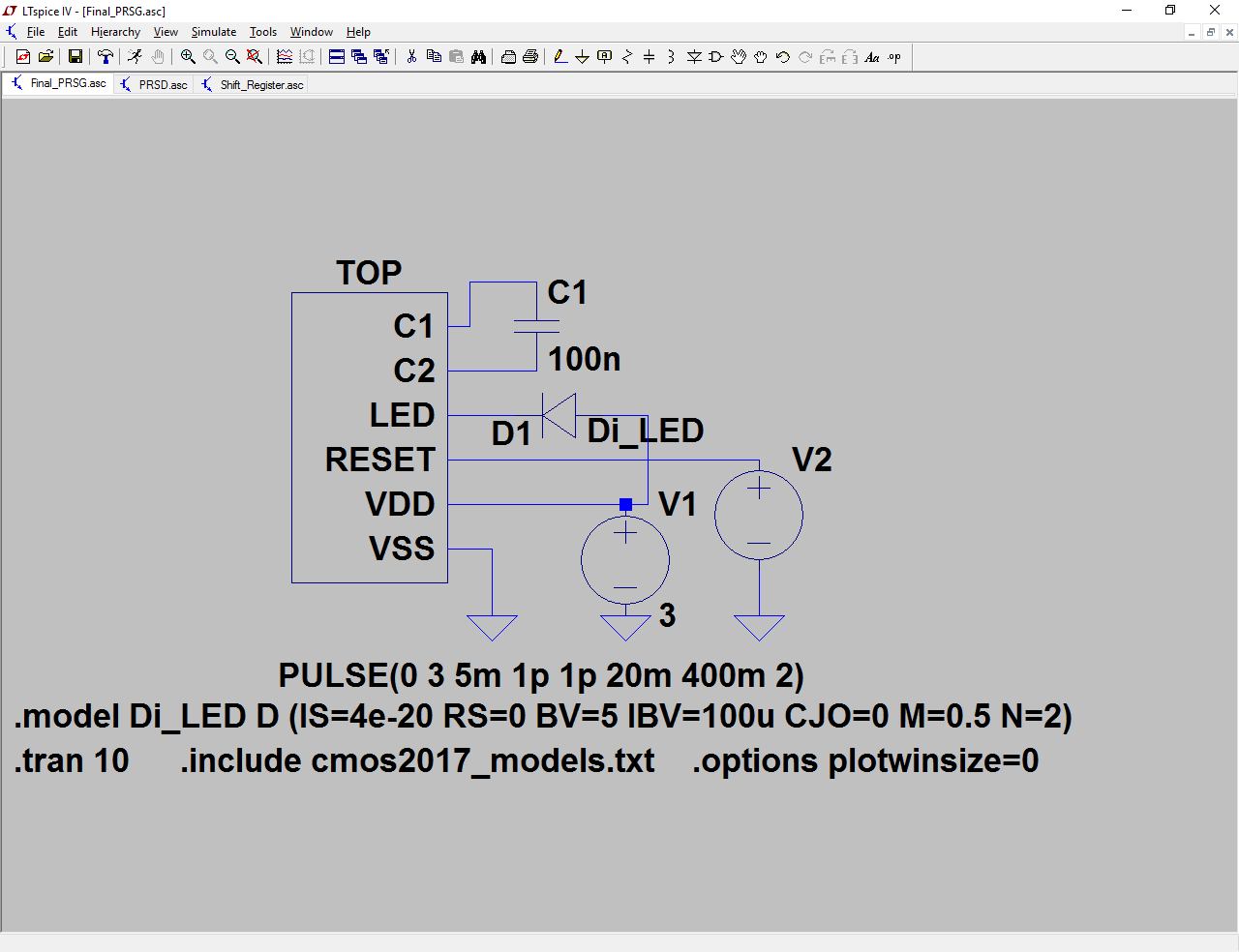


Figure 27: Top Level Schematic

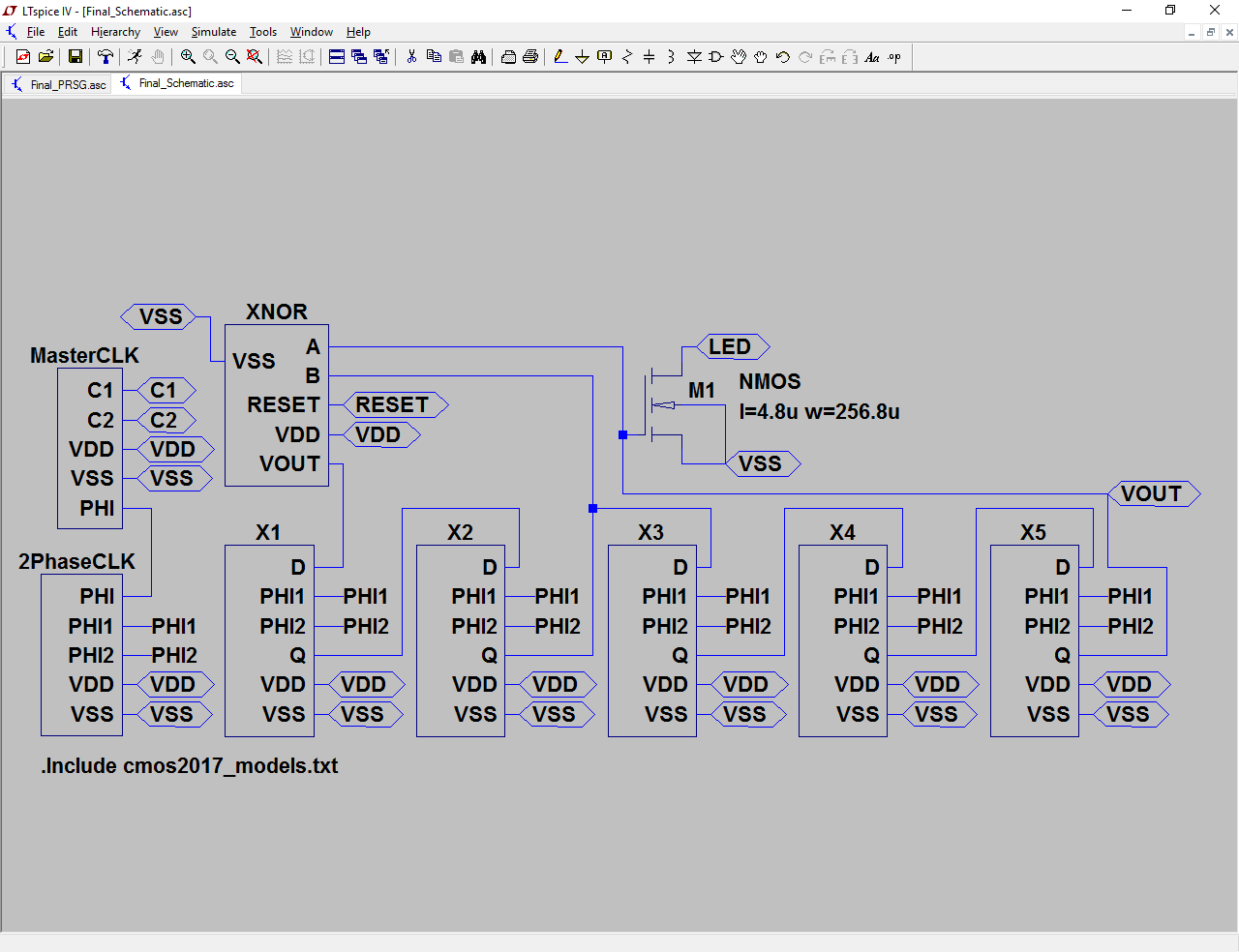


Figure 28: Complete Top Level Circuit Schematic

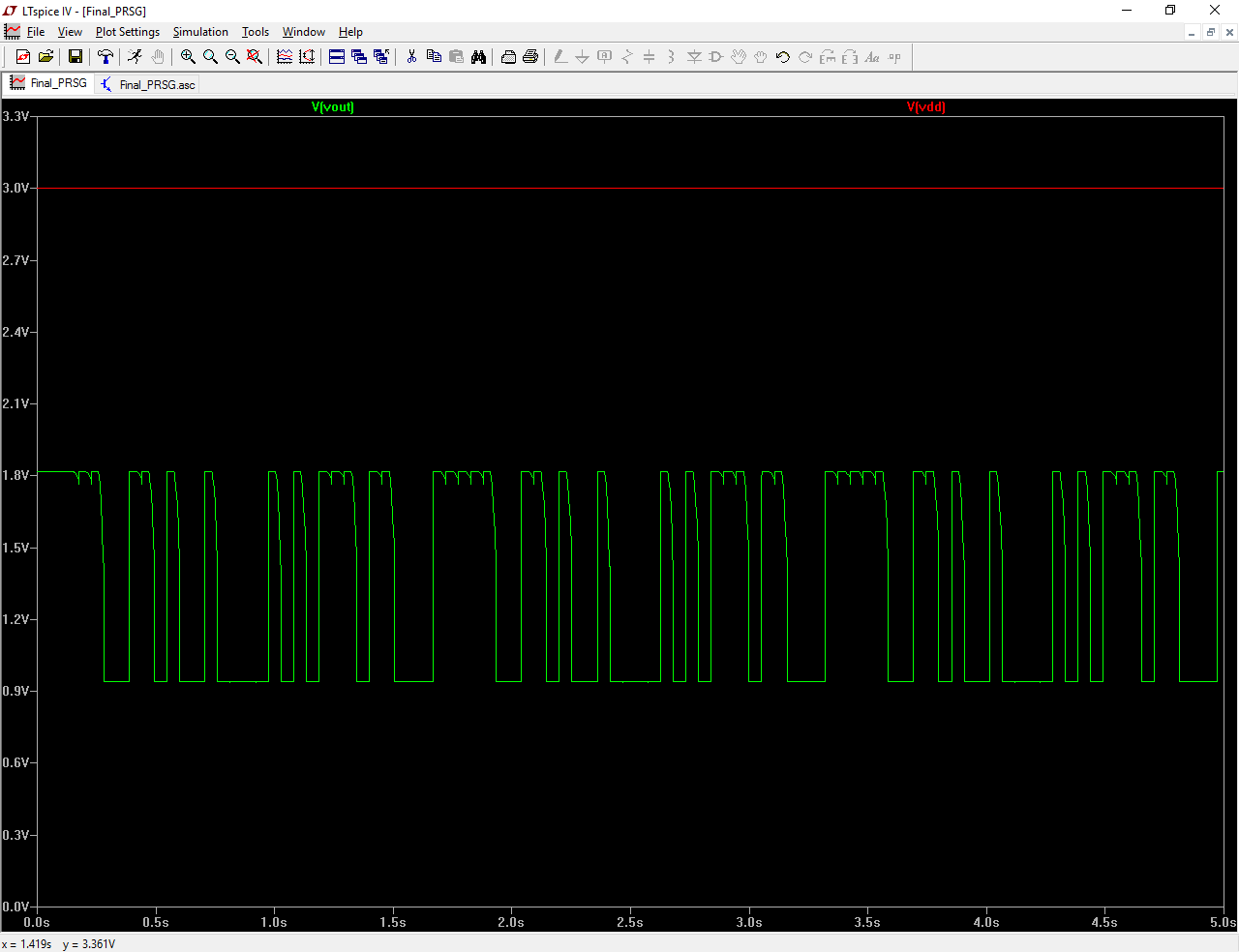


Figure 29: PRSG Output SPICE Simulation

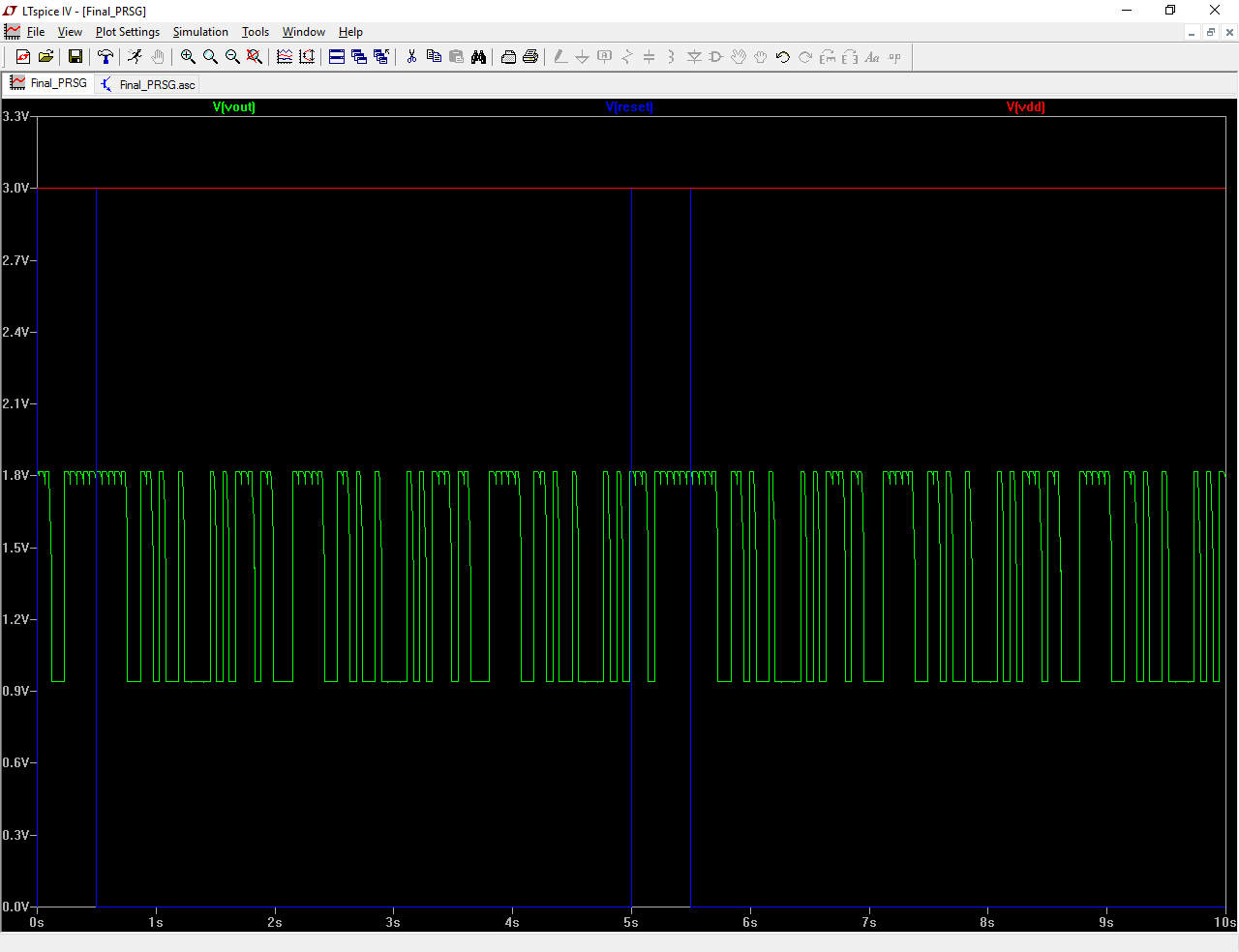


Figure 30: PRSG Output with RESET SPICE Simulation

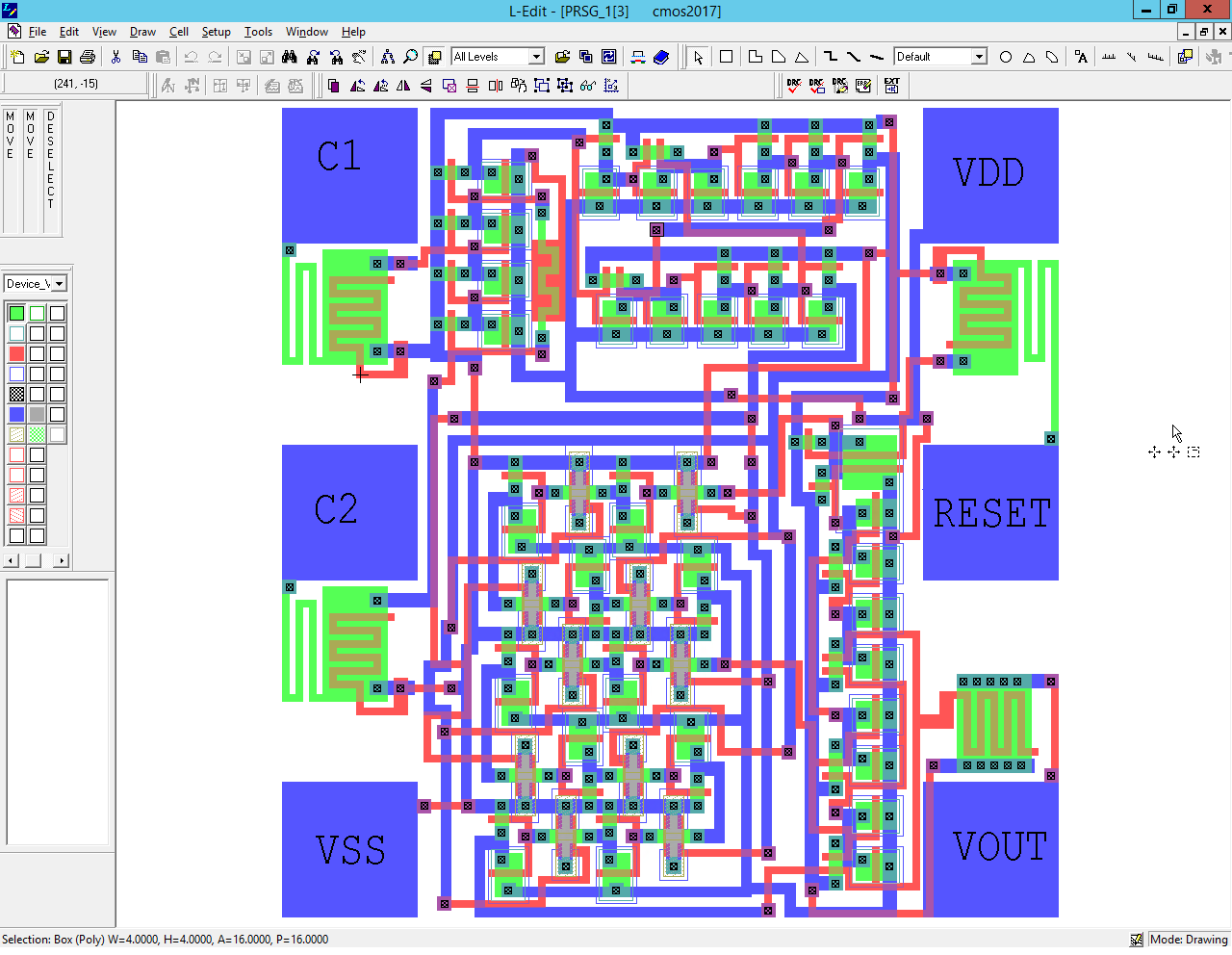


Figure 31: Final PRSG Layout

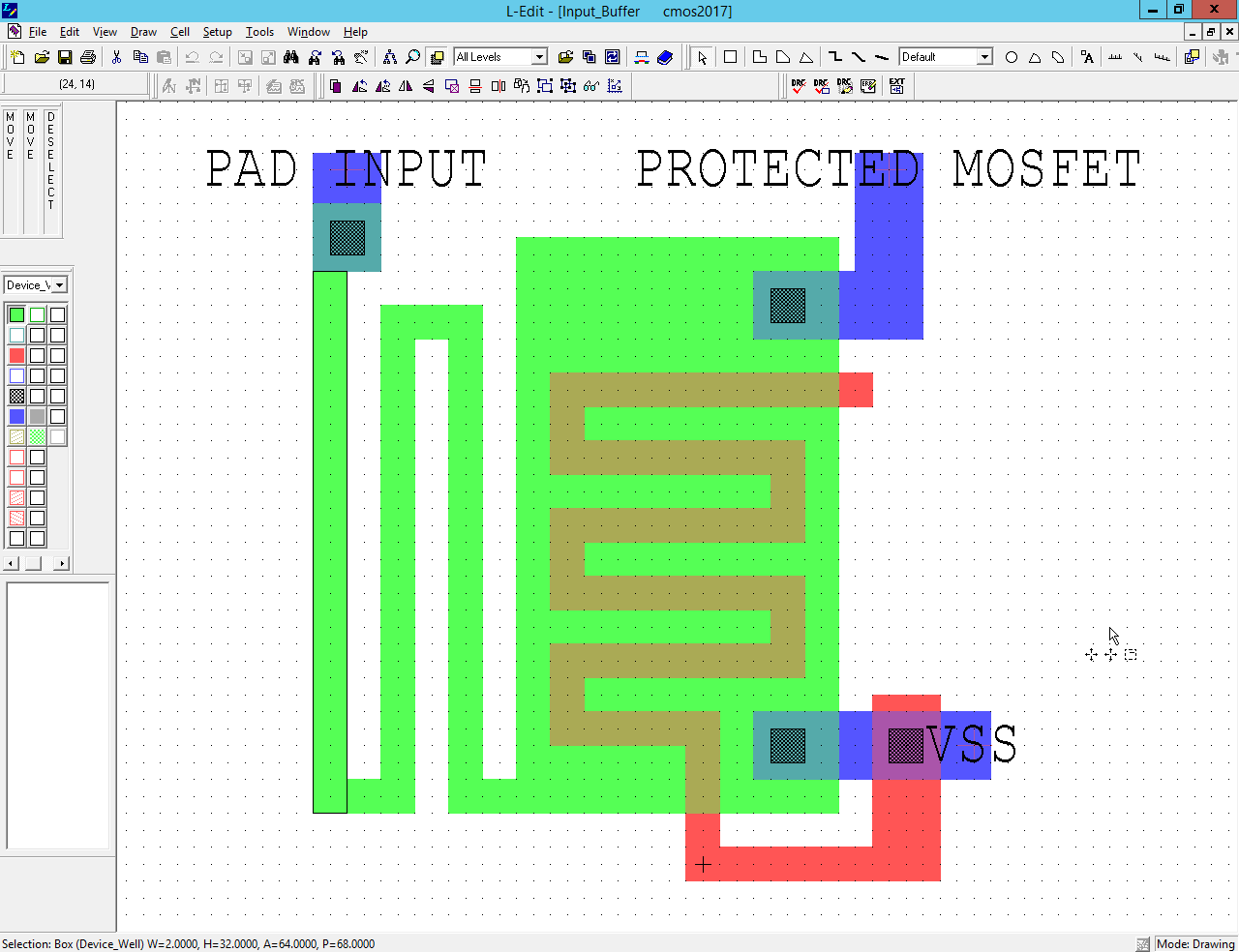


Figure 32: Input Protection Layout

Please check Appendix A for the DRC results of full, complete layout.

Please check Appendix B for the LVS results of full, complete layout.

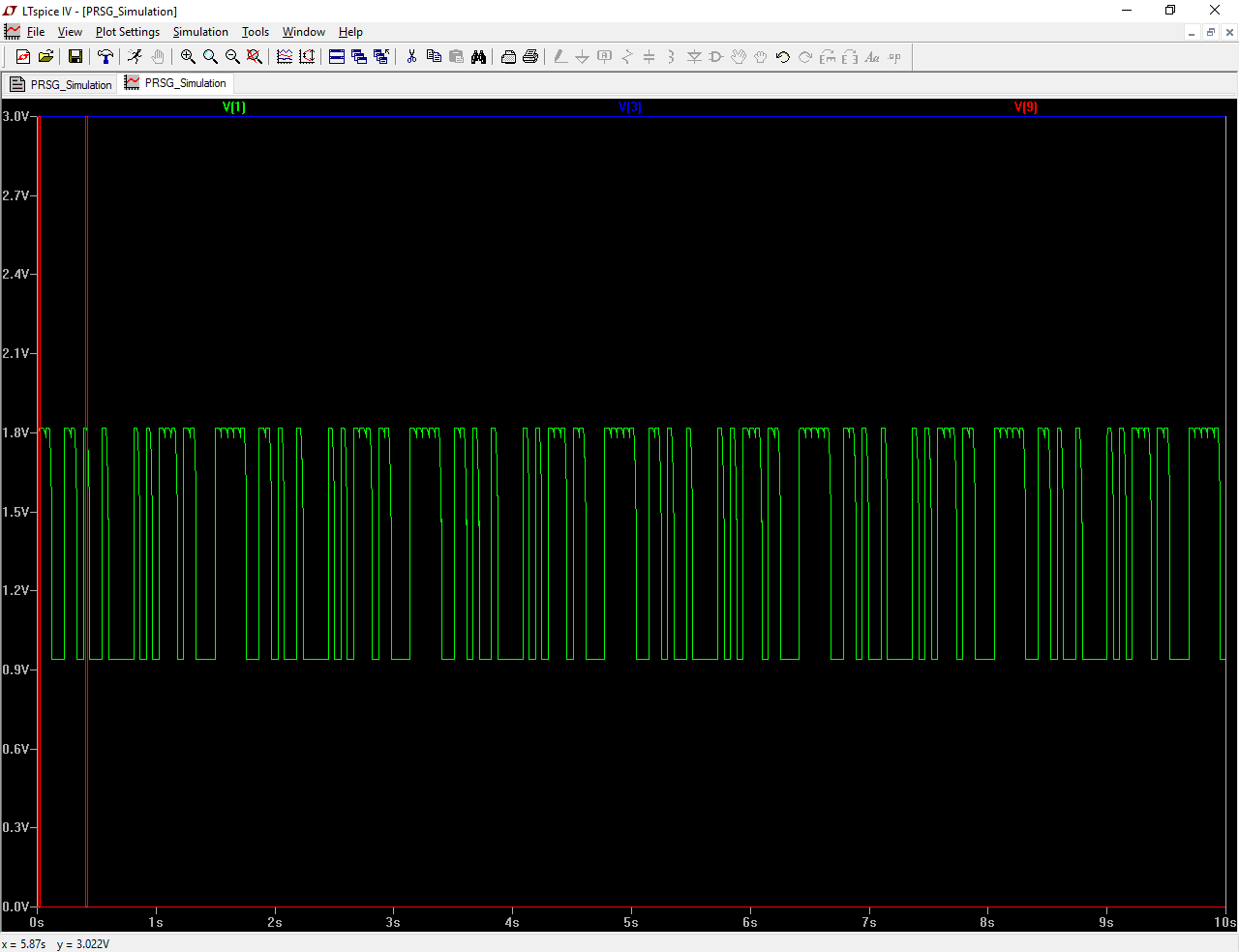
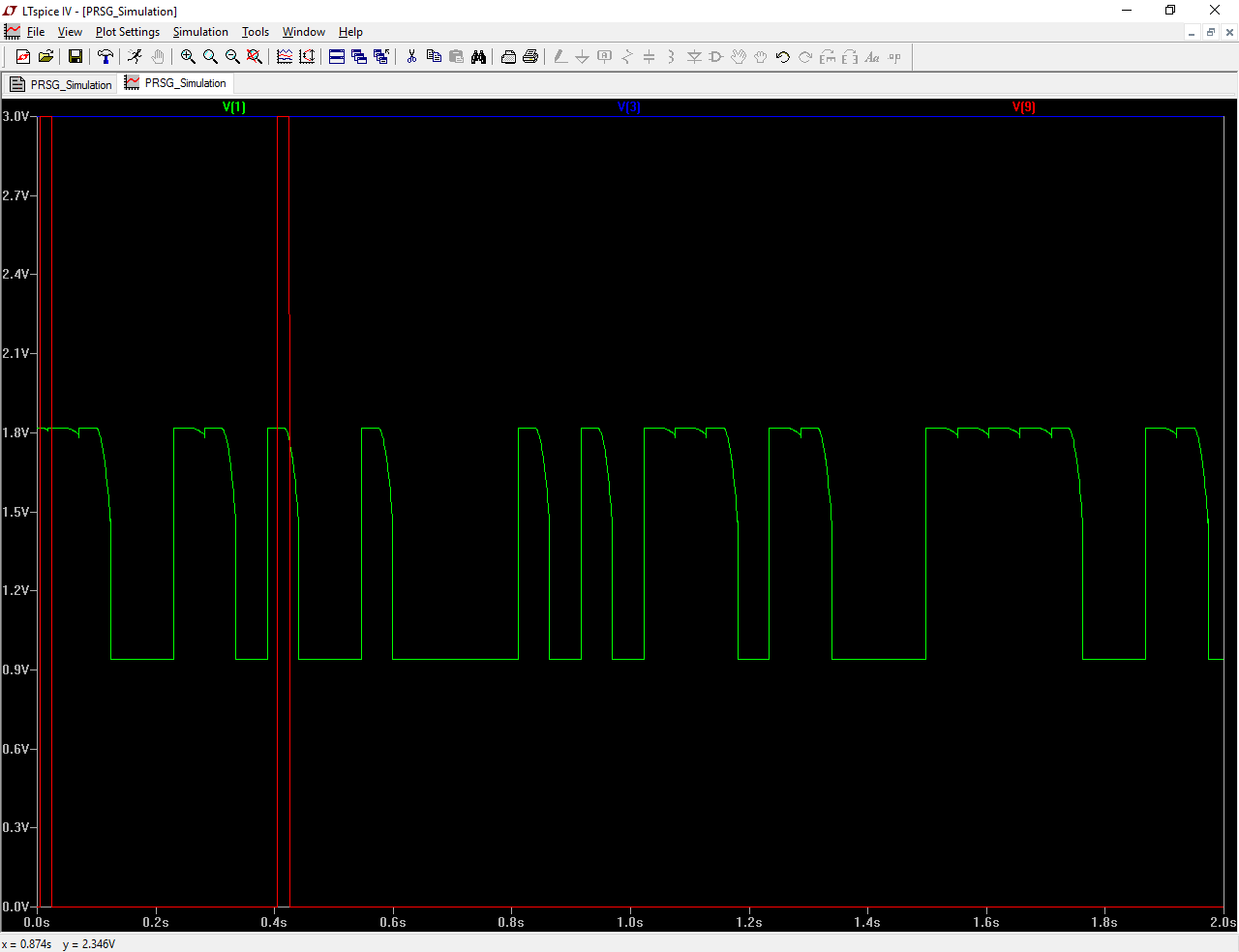


Figure 33: Full, Complete Final Layout SPICE Simulation for 10s

The outputs of schematic and extracted PRSG are identical; differences/accuracy, if any, may arise from the transient computation of the voltages. The figures below directly compare the extracted circuit to that from the schematic. Aside from the slight output shift, the rest of the waveform is identical.

In order to minimize the layout are size, few key steps were taken during the progress of this project. One of the methods used was during the designing each of the blocks; picking the smallest MOSFET lengths and widths, while having the simulation output a desirable waveform. It was also key to try and rid of as many NOR gates as possible, and opt of the circuits NAND gates equivalent. Similarly, it was useful to use nMOS transistors instead of pMOS.



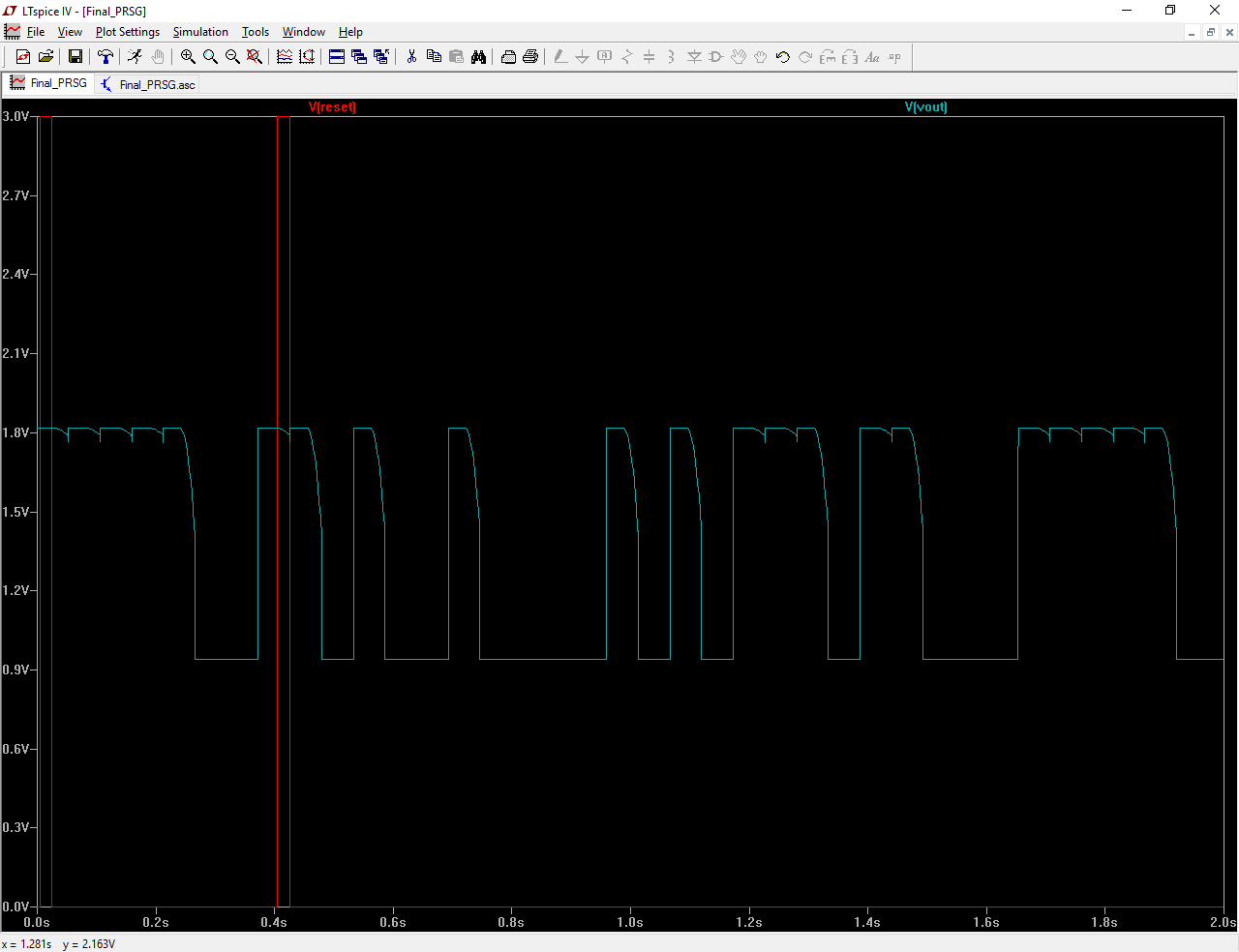


Figure 34: Full, Complete Final Layout (Green) and Schematic (Cyan) Comparison SPICE Simulation for 2s

**APPENDIX A**

DRC by Tanner Research's L-Edit Version 9.00

Cell: PRSG\_1

Bin Size = 200000.0000 locator units

0 errors.

0 warnings.

Layer Derivation Statistics

Source\_Drain 1.4210 sec (47.37%)

poly\_contact 0.0160 sec (0.53%)

active\_contact 0.0160 sec (0.53%)

p-well 0.0150 sec (0.50%)

channel 0.0000 sec (0.00%)

pdiff 0.0000 sec (0.00%)

DRC Statistics

Req. Metal Surrounding Contact 0.1250 sec (4.17%)

p-well surrounding nMOS 0.0630 sec (2.10%)

Poly To Poly Spacing 0.0160 sec (0.53%)

Minimum Source Drain Width 0.0160 sec (0.53%)

Required Poly around Poly Contact 0.0160 sec (0.53%)

Poly To Active Spacing 0.0150 sec (0.50%)

Minimum Poly Extension Over Field 0.0150 sec (0.50%)

Minimum active width 0.0000 sec (0.00%)

n-well surrounding pMOS 0.0000 sec (0.00%)

Minimum metal width 0.0000 sec (0.00%)

p+ surrounding pdiff 0.0000 sec (0.00%)

n+ to p+ spacing 0.0000 sec (0.00%)

Contact Width 0.0000 sec (0.00%)

Contact To Contact Spacing 0.0000 sec (0.00%)

Channel To Active Contact Spacing 0.0000 sec (0.00%)

Active To Active Spacing 0.0000 sec (0.00%)

Metal To Metal Spacing 0.0000 sec (0.00%)

Active Surrounding Active Contact 0.0000 sec (0.00%)

Exact Passivation Opening Size 0.0000 sec (0.00%)

Metal Surrounding Passivation Cut 0.0000 sec (0.00%)

Minimum poly width 0.0000 sec (0.00%)

Select layer generation elapsed time: 00:00:00 (0.00%).

Merge/Boolean layer generation elapsed time: 00:00:02 (66.67%).

DRC rule checking elapsed time: 00:00:00 (0.00%).

Total DRC elapsed time: 00:00:03.

**APPENDIX B**

File written by LVS 9.00 as a result of: "W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output.vdb" on Tue Mar 21 16:11:14 2017

Command line:

lvs W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_2.spc W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_1\_EXTRACT\_Protection\_Pads.txt -o W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output.out -l W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output.lst -t W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output\_flat.sp -h W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output\_flat.spc -mm ALL -r ALL -pspice -nrcl -c2 -dg5.000 -vfpar

Engine configuration report:

Layout netlist file.............................................. W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_2.spc

Layout netlist file format....................................... P-Spice

Schematic netlist file........................................... W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_1\_EXTRACT\_Protection\_Pads.txt

Schematic netlist file format.................................... P-Spice

Consider Bulk nodes.............................................. ON

Consider Resistors as polarized elements......................... OFF

Consider Capacitors as polarized elements........................ OFF

Consider Inductors as polarized elements......................... OFF

Merge series and parallel R...................................... OFF

Merge series and parallel C...................................... OFF

Merge series and parallel L...................................... OFF

Merge parallel M................................................. ALL

Merge parallel D................................................. OFF

Merge parallel B................................................. OFF

Merge parallel J................................................. OFF

Merge parallel Z................................................. OFF

Merge parallel Q................................................. OFF

Merge series MOSFETs............................................. ON

Find series MOSFETs that differ in order......................... OFF

Remove shorted devices........................................... OFF

Remove disconnected devices...................................... OFF

Fast Iteration................................................... OFF

Parameter comparison threshold for MOSFET GATE LENGTHS........... 5%

Parameter comparison threshold for MOSFET GATE WIDTHS............ 5%

Parsing file W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_2.spc...

Warning: PRSG\_2.spc(18): Implicit .model definition PMOS

Warning: PRSG\_2.spc(88): Implicit .model definition NMOS

Flattening netlist...

Parsing file W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_1\_EXTRACT\_Protection\_Pads.txt...

Including file W:\Desktop\ELEC4609\_PRSG\_D\cmos2017\_models.txt

Flattening netlist...

Device PRSG\_2.spc PRSG\_1\_EXTRACT\_Protection\_Pads.txt Status

--------------- --------------- --------------- ---------------

M\_NMOS 50 50

M\_PMOS 35 35

------------ ------------

Total elements 85 85

Total nodes 50 50

Single-pin nodes 1 1

Merging devices...

Eliminated nothing.

Writing PRSG\_2.spc to flat spice file: W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output\_flat.sp

Writing PRSG\_1\_EXTRACT\_Protection\_Pads.txt to flat spice file: W:\Desktop\ELEC4609\_PRSG\_D\PRSG\_Output\_flat.spc

Merging series MOSFETs...

PRSG\_2.spc: Merged 14 series MOSFETs (eliminating 7 nodes).

PRSG\_1\_EXTRACT\_Protection\_Pads.txt: Merged 14 series MOSFETs (eliminating 7 nodes).

Device PRSG\_2.spc PRSG\_1\_EXTRACT\_Protection\_Pads.txt Status

--------------- --------------- --------------- ---------------

2xSERIES\_M\_NMOS 6 6

2xSERIES\_M\_PMOS 1 1

M\_NMOS 38 38

M\_PMOS 33 33

------------ ------------

Total elements 78 78

Total nodes 43 43

Single-pin nodes 1 1

Iterating...

5% done.

10% done.

15% done.

20% done.

25% done.

30% done.

35% done.

40% done.

45% done.

50% done.

55% done.

60% done.

65% done.

70% done.

75% done.

80% done.

85% done.

90% done.

95% done.

100% done.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* FINAL RESULT \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Note: Series MOSFETs have been merged.

Lengths and widths not considered during this process.

Circuits are equal.

Run time: 0:01 (min:sec)

0 error(s), 2 warning(s)